

Radiation Tolerant Linear Laser Driver IC

Reference and Technical Manual

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January 2002

Version 4.1

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Introduction

A new version of the Linear Laser-Driver IC has been designed by the CERN EP Microelectronics group, and implemented in a radiation tolerant CMOS technology. The IC is targeted for the transmission of analogue data from the CMS central tracker detectors (silicon microstrip) to the front-end digitiser cards. The new ASIC drives a group of three laser-diodes converting the analogue data produced by the front-end APV chips into amplitude modulated optical signals. Each laser-driver in the IC contains a programmable current source allowing independent biasing of any of the three laser-diodes in its linear region of operation. The same component is well suited to drive the less demanding digital optical links, for TTC signal distribution.

This document is intended to provide a functional and physical description of the Linear Laser-Driver IC.

CMS TRACKER READ-OUT ARCHITECTURE OVERVIEW

The CMS Tracker read-out architecture is described in [1], [2] and [3]. In order to put the Linear Laser-Driver IC into context, we present in this introduction an overview of the CMS tracker read-out architecture. The description done here is brief, simplified and it does not pretend to represent accurately the final system implementation.

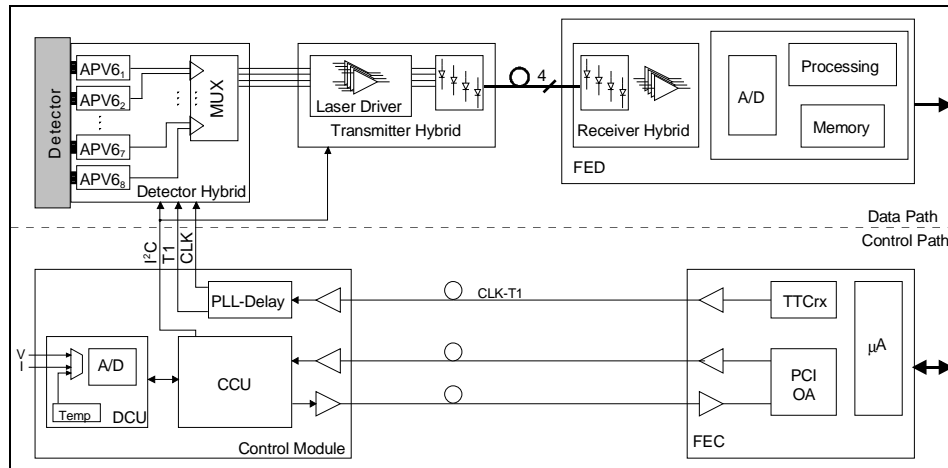


Figure 1 General tracker read-out architecture

Figure 1 represents the general read-out architecture that will serve the CMS tracker. On the occurrence of a first level trigger, the analogue signals that have been previously processed and pipelined by the APV front-end ICs are sent to the transmitter hybrid by passing through the external multiplexer IC (MUX in Figure 1). The main function of this IC is to time division multiplex the analogue data from six APVs into three communication channels. Since the data rate at the output of each APV is 20 Mbaud, each communication channel carries a 40 Mbaud data stream. Communication between the two hybrids is made using short lengths of twisted pair copper cables (0-30 cm) of 100 Ω characteristic impedance. In the transmitter hybrids, the Linear Laser-Driver IC and the laser-diodes convert the electrical signals

into optical signals. No special modulation scheme is used and the analogue data is transmitted as amplitude modulated optical signal. Optical fibres are used to send the data to the Front-End Digitiser (FED) modules outside the detectors. Since each APV IC serves 128 detector channels, a single optical fibre link is used to transmit data from 256 channels. In the system there will be approximately a total number of 12 million detector channels (Si-strips) corresponding to 50 thousand optical read-out links.

Laser-Driver IC Specifications

The data transferred from the detector to the FED modules is in the form of pulse amplitude modulated analogue signal. In order to achieve the required system signal-to-noise ratio the electrical-to-optical conversion has to be made with minimum noise and non-linear distortion. An objective for the whole communication channel – from the APVs outputs to the digitising modules – is to achieve a performance equivalent to that of a 7-bit digital system. Each link element should thus exceed this performance. The goal fixed for the Linear Laser-Driver IC was to attain an 8-bit equivalent performance. Taking into account this requirement and the modularity of the data path, the following specifications were set [4] [5]:

- ◆ Technology: 0.25 μm CMOS (using radiation tolerant layout technique [6] [7])
- ◆ Modularity: Three channels per IC
- ◆ Input impedance: 100 Ω (to be set by external resistor)
- ◆ Input signal (relative to midpoint $V_{\text{dd}}/2$):
 - ± 300 mV differential (for specified linearity)
 - ± 500 mV differential (maximum)
 - ± 250 mV common mode range
- ◆ Trans-conductance: 5 / 7.5 / 10 / 12.5 mS (pre-settable)
- ◆ Pre-bias current: 0-55 mA (current sink)
- ◆ Dynamic range: 8 bits (50 dB)
- ◆ Linear deviation: < 1% (over the operation range)
- ◆ Equivalent input noise: < 0.8 mV
- ◆ Bandwidth: > 100 MHz
- ◆ Settling time: < 10 ns to within 1% of the final value
- ◆ Cross-talk: < -60 dB
- ◆ Delay uniformity: < 1 ns
- ◆ Power supply (V_{dd}): 2.5 V ($\pm 10\%$)
- ◆ Power dissipation per channel:
 - 30 mW (at minimum pre-bias current)
 - 200 mW (at maximum pre-bias current)
- ◆ Others:
 - I2C interface (SEU robust)
 - Individual programming of each channel
 - Individual per channel power-down function
 - Start-up mode for digital link

The Linear Laser-Driver IC

In this chapter the Linear Laser-Driver IC architecture, functionality, circuits and physical implementation are described.

ARCHITECTURE

The block diagram of the Linear Laser-Driver IC is represented in Figure 2. The IC is made of three Laser-Drivers (LD) and of an I²C interface. Each driver takes a differential input voltage and converts it into a unipolar current that is used to modulate an external laser-diode. The analogue input signal is transmitted to the IC using a 100 Ω twisted pair cable. To avoid reflections of the signal — and consequently bad settling times — it is important to terminate the cable in its characteristic impedance. Since, in the IC technology used, there were no precision resistors available, it is necessary to terminate the cable using an external 100 Ω precision resistor as close as possible to the IC.

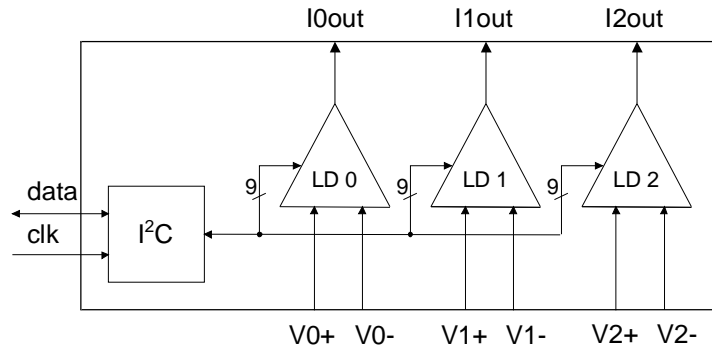


Figure 2 Linear Laser-Driver IC block diagram

Besides signal modulation each driver also generates a *dc* current that is used to bias the external laser-diode. This current allows the laser-diode to be operated above threshold in the linear region of its characteristics. As shown in Figure 3 the modulation current and the bias current are independently processed and summed in the output node. Device ageing and performance degradation due to radiation cause the laser-diodes threshold currents to change with time. To compensate for these variations the laser-diode bias current was made programmable through the I²C interface. Since each device in the group will have different thresholds and might age differently, the bias current produced by each driver was made individually programmable.

Monolithic arrays of laser diodes are also being considered as candidate devices to be used inside the tracker. They are normally manufactured as either common-cathode or common-anode arrays. Therefore, the Laser Driver IC must be able to either source the *dc*-current (*source-mode* of operation) or sink it (*sink-mode* of operation). The *sign* bit (shown in Figure 3) is provided for this purpose. The denomination of non-inverting and inverting inputs is opposite in the two modes of operation (the input that is non-inverting in *source-mode* becomes inverting in *sink-mode* and vice-versa). The driver output should be connected to the anode of the

laser diode, when operating in source mode, and to its cathode, when operating in sink mode.

Gain variability and enabling/disabling of individual channels is also provided, and can be controlled by the I2C interface. The driver gain variability allows an optimum equalisation of the analogue transmission chain. The power down function allows reducing the power consumption and noise of non-used or defective channels.

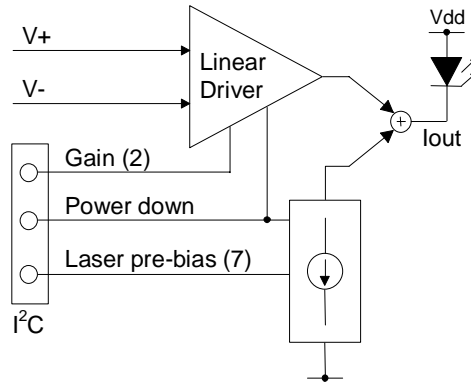


Figure 3 Laser-Driver block diagram and diode connection.

FUNCTIONAL

Laser-Driver

Each Laser-Driver in the IC typically works with an input differential voltage between ± 300 mV. Within this range the integral non-linearity of the output current is guaranteed to be less than 1%. Each driver can however accept differential input voltages up to ± 500 mV. Above this limit, the output current is not specified and can eventually saturate. The driver trans-conductance is pre-settable among four different values (5, 7.5, 10 and 12.5 mS), by acting on the 2 gain bits. This results in an output current range of ± 2 , ± 3 , ± 4 and ± 5 mA respectively, when the input differential voltage changes from -400 mV to $+400$ mV. The laser-diode bias current is generated inside each Laser-Driver. This current is programmable through the I²C interface between 0-55 mA in steps of 0.45 mA. (7-bit resolution).

The IC operates between 0-2.5V power supplies. For this power supply the common mode input range is defined as $1.25V \pm 0.25V$. Within this common mode range the IC behaves according to the specified performance.

I²C Interface

The Linear Laser-Driver IC implements a standard I²C protocol [8]. The IC contains four internal 7-bit registers. The first three read/write registers are used to independently program the external laser-diodes bias-currents, with 7-bit resolution. The fourth register contains 6 read/write bits which are used to program the gains of the three Laser Driver channels (2-bits per channel). The additional read-only bit contains a flag that is activated when an SEU event is detected (SEU flag).

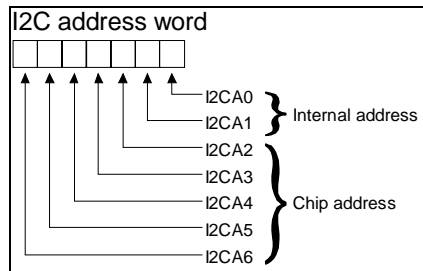


Figure 4 I²C address decoding

The IC is addressed using a seven bit address number (I2CA6 to I2CA0). Bits I2CA1 and I2CA0 are used to address the four internal programming registers (see Figure 4). Bits I2CA6 to I2CA2 are the IC address, which must be configured using the external ASIC inputs with the same names. It should be noted that those inputs contain internal pull-down resistors. They should be hard-wired to the positive power supply for logical '1' or left open for logical '0'. The inputs are not latched by the IC logic and, consequently, they should remain stable during operation.

The laser-diodes bias currents are controlled by writing in the three bias-current programming registers. These registers accept the standard 7-bits of data from the I²C interface (Figure 5). The bias current is approximately given by the programmed number times 0.45 mA (LSB).

The bias-current programming registers also control the power-down function for each individual channel. When the seven bits are simultaneously set to zero, the power-down function is activated. This conventional configuration of bits in a register disables the corresponding driver, thus reducing the power consumption and noise of a non-used or defective channel.

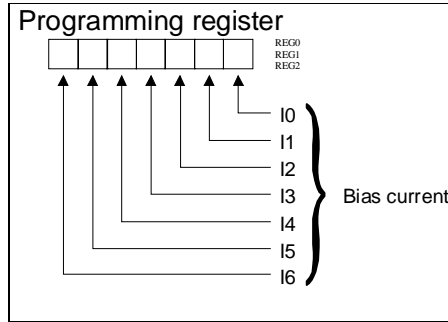


Figure 5 Bias-current programming register

Six bits in the gain programming register (Figure 6) determines the gain of the individual channels. Two bits per channel allow choosing the gain among the four pre-settable values, according to the following table

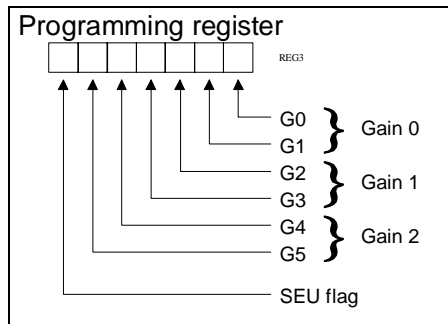


Figure 6 Gain programming register

Gain bit-1	Gain bit-0	Gain value
'0'	'0'	5.0 mS
'0'	'1'	7.5 mS
'1'	'0'	10.0 mS
'1'	'1'	12.5 mS

Table 1 Gain values

The Laser Driver IC is intended to operate in a harsh radiation environment, and it is therefore susceptible to Single Event Upsets (SEU) which could eventually upset the contents of the I2C interface registers. The interface robustness to SEU is increased

by tripling all the logic and all the registers, and by using a majority voting decision scheme. This means that the content of the registers is actually stored in three memory locations, which are constantly compared bit by bit. The value which is actually passed through (and which determines the behaviour of the analogue blocks) is the one which is stored in at least two of the three memory locations. As an additional precaution, the event of one memory location being corrupted in any of the register triples is detected and flagged in the SEU bit (SEU flag). The status of the SEU flag indicates if such an event has occurred ('1') or not ('0'). The strategy for scanning the SEU flag and eventually reprogramming the registers is to be defined by the user.

Reset Logic

The Laser Driver IC contains two reset inputs: the power-on reset input (PONb) and the system reset input (RESb). Both of them work on a negative logic (b=bar). The PONb input must be connected to an external RC network (as shown in Figure 8). The time constant $\tau=1/RC$ must be greater than the switching-on time of the power supply.

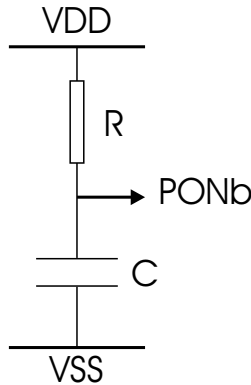


Figure 7 Power-on reset network

The system reset input can be optionally connected to a remote control. An internal pull-up resistor insures that RESb stays high in case it is not connected.

On occurrence of a reset (power-on or system reset), all the registers are set to their initial values. The initial value of the bias-current programming registers can be pre-set by connecting the inputs DRES4, DRES5, DRES6. These inputs are common to the three driver channels and determine the initial value of the 3 most significant bits of the programming registers (I4 to I6). The 4 least significant bits are reset to logical '0's. It should be noted that these inputs contain internal pull-down resistors. Thus it is necessary to connect them to positive power supply to program a logical '1', while they can be left open to program a logical '0'. For the analogue links, it is convenient that the drivers stay disabled when the system is powered or reset, until the first I2C write operation. Therefore, the DRES inputs might simply be left unconnected. For the digital links, however, the lasers *must* be active at system start-up or reset, to insure the possibility of communication between the detector front-ends and the outside world. In this case, the initial bias-current of the lasers must be configured using the DRES inputs. The gain programming register is in all cases reset to all '1's (maximum gain).

LASER-DRIVER CIRCUITS

IC Bias

A simplified schematic of the IC bias circuit is represented in Figure 8. This consists of a standard *bootstrap reference* [9], where the reference current I_{ref} is approximately given by V_{T1}/R and the corresponding reference voltage V_{ref} is used to bias the IC. The left-hand part of the circuit (dotted) insures that the circuit is correctly bootstrapped, but is cut-off during normal operation. This circuit technique can be implemented in a full CMOS technology and has the advantage of being relatively immune to power-supply noise.

To minimise cross talk among the different channels each driver in the IC contains its own bias circuit. This results in an increase of the ASIC power consumption. However, the incurred power penalty is small since the bias circuit contributes only with a small fraction to the total power consumption.

A power-down function is also implemented in this circuit by the switches shown in Figure 8. Since the driver works by duplication and multiplication of the reference current, once this current is forced to zero no power is available to the driver circuits reducing the power consumption essentially to zero. The power-down function is controlled by the I²C interface as explained in the previous section (see I²C Interface).

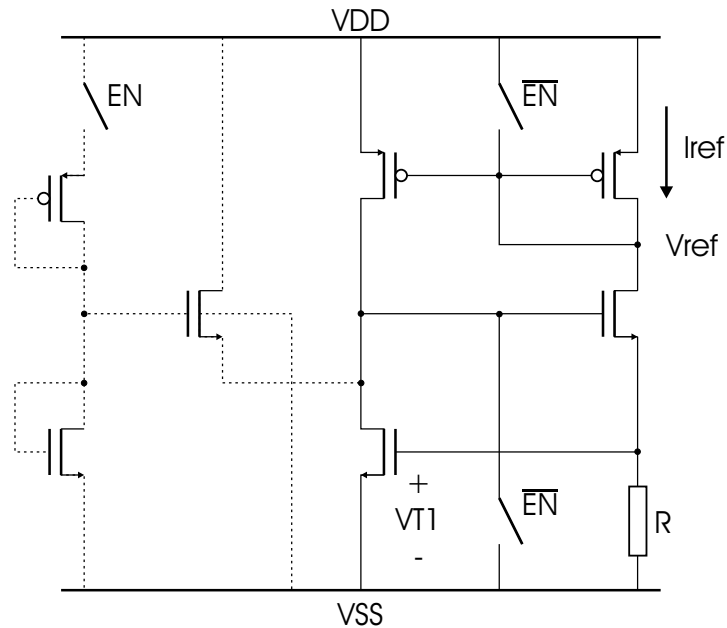


Figure 8 Bootstrap current reference

Laser-Diode Bias Circuit

The laser-diode bias circuit consists of an array of 127 elementary current sinks (Figure 9). As mentioned before, this circuit allows to bias the laser-diode in its linear region of operation and to compensate for device-to-device variations, device ageing and device performance degradation due to radiation. The elementary current sinks are switched-on and off, according to the contents of the programming registers. A

unipolar current can be programmed whose module is linearly variable between 0 mA and 55 mA.

The elementary current sinks have been implemented using the regulated-cascode technique [10]. This scheme has the advantage of providing relatively high output impedance, while the compliance output voltage and the power-supply rejection-ratio are still compatible with the specification. The reference voltages *Ref1* and *Ref2* are generated by two independent reference circuits of the kind described in the previous section (see IC Bias).

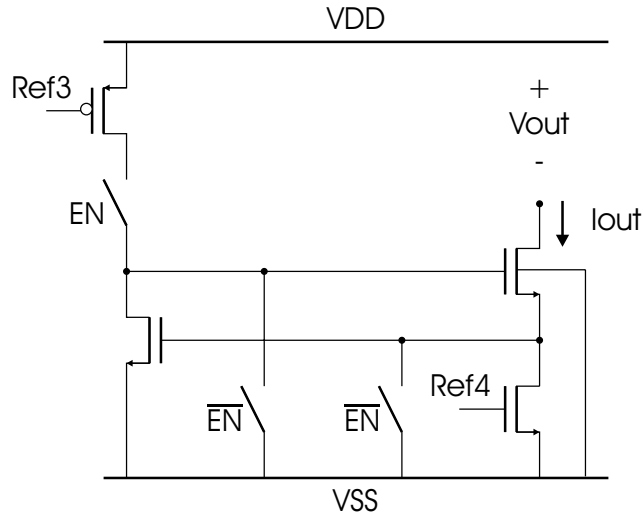


Figure 9 Laser-diode bias circuit

Linear-Driver

The Linear-Driver is the part of the Laser-Driver that is responsible for signal modulation of the laser-diode. This is the only part of the circuit with currents actually switching during normal operation¹.

A simplified schematic of the Linear-Driver is shown in Figure 10. The Linear-Driver consists of a differential-pair preamplifier (left-hand side of the schematic) and a push-pull output stage (right-hand side of the schematic). The differential-pair amplifies the input differential voltage and converts it in a differential current, which is amplified and summed by the output stage. The differential-pair, compared with alternative design solutions, is conceptually simple and offers good dynamic and noise performance at limited power dissipation. The PMOS version is bulk-effect-free, thus allowing a larger input common-mode range.

The push-pull output stage provides gain variability. The output stage actually consists of three stages in parallel, with binary weighed gain and current summation at the output. The first stage (gain = 2) is always active, whereas the second and third stages (gain = 1 and 2) can be switched on and off, according to the contents of the gain programming register. The overall gain of the output stage can be 2, 3, 4 or 5. This has to be multiplied with the gain of the differential-pair pre-amplifier of 2.5 mS.

¹ The digital logic is quiet during data acquisition. The noise interference should be kept to a minimum during this operation period.

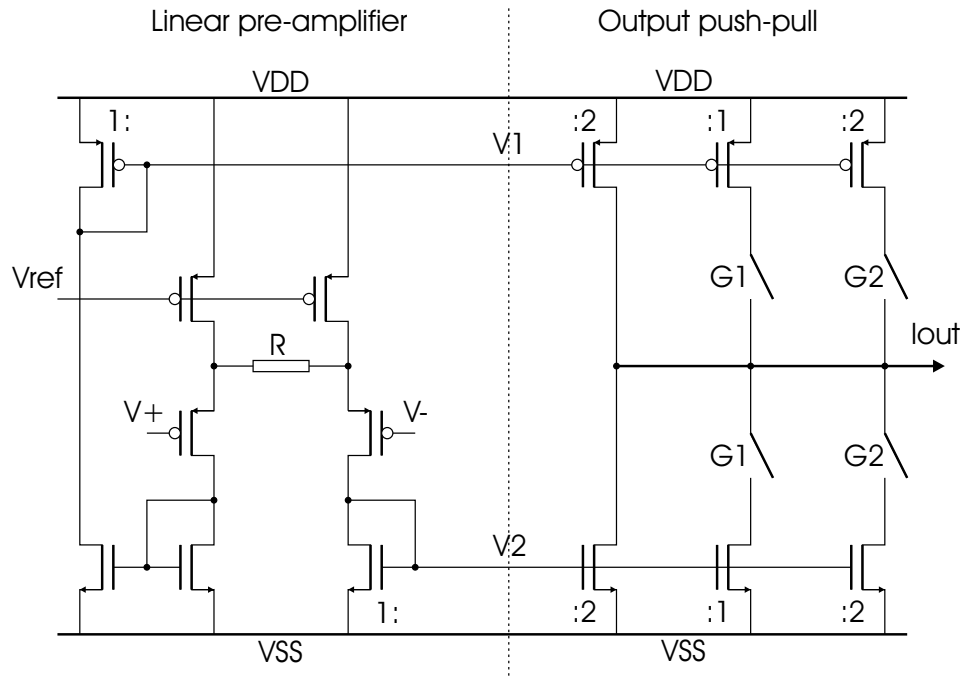


Figure 10 Linear-Driver

The overall current absorbed by the circuit and laser-diode is kept constant (i.e. independent from the input signal), in order to limit as much as possible current fluctuations and noise induced in the global power-supplies. The power dissipation of the Linear-Driver is below 30 mW per channel.

The required linearity is obtained with a combination of two source-degeneration methods: a parallel source-degeneration resistor, and a source-bulk cross-connection between the transistors of the differential-pair (as highlighted in Figure 12). The combination of these two methods allows keeping the degeneration resistor to a value compatible with the required input common-mode range. Source-degeneration methods apply local feedback to achieve the required linearity. Although global feedback can be a more efficient means of linearisation it is also potentially more susceptible to produce stability problems due to output loading effects. Additionally, global feedback is difficult to apply to a differential structure such as the one used. For these reasons, local linearisation was preferred in the design of the Linear-Driver.

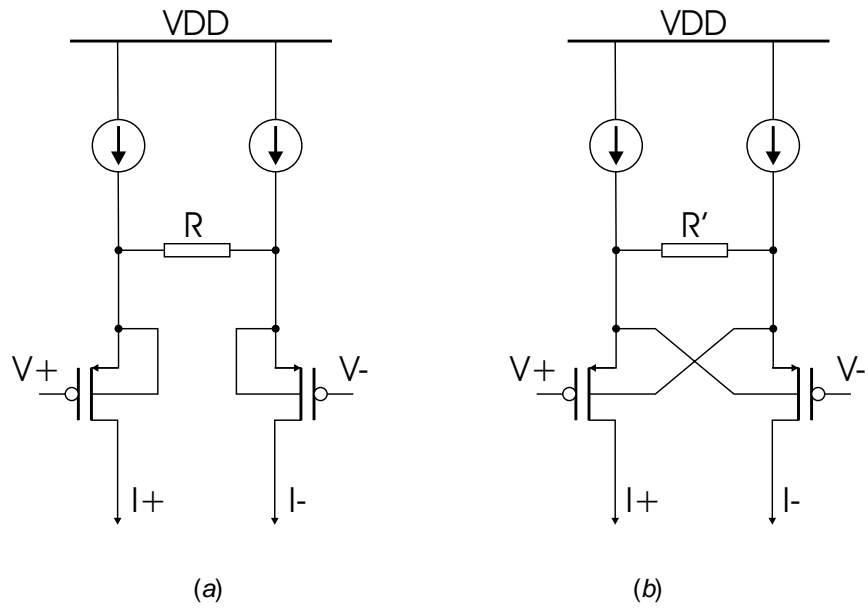


Figure 11 PMOS differential pair input stage, with parallel source degeneration resistor (a and b) and with cross-connected sources and bulks (b only).

As discussed before input termination has to be made externally to the circuit by means of an $100\ \Omega$ resistor as close as possible to the IC. Good input matching is important to avoid the degradation of the input signal settling time due to input signal reflections.

PHYSICAL IMPLEMENTATION

The Linear Laser-Driver IC was fabricated in a standard commercial 0.25µm CMOS process. The ASIC dimensions are 2.00 mm × 2.00 mm. We intend to package the device in LPCC-32 packages (dimension: 5mm x 5mm). **Error! Reference source not found.** shows the package pinout.

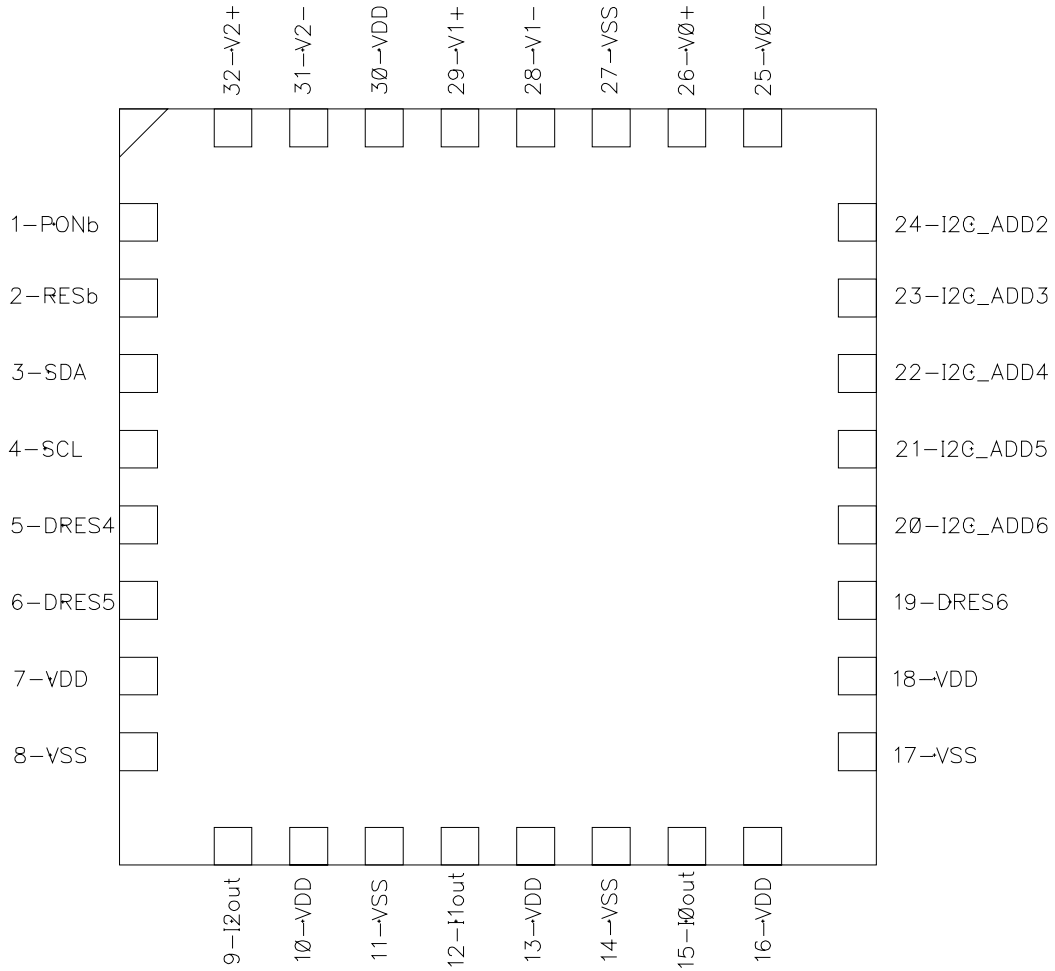


Figure 12 Linear Laser-Driver package (LPCC-32, 5mm x 5mm).

IC Signals

Pin Number	Pin Name	Pin Type	Description
1	PONb	Input	Power-on reset (to external RC network)
2	RESb	Input	System reset (internal pull-up)
3	SDA	Bidirectional	I2C serial data (to external pull-up)
4	SCL	Input	I2C serial clock
5	DRES4	Input	Registers bit 4 value at system reset (internal pull-down)
6	DRES5	Input	Registers bit 5 value at system reset (internal pull-down)
7	VDD	Power	Power supply
8	VSS	Power	Ground
9	I2out	Output (analog)	Channel 2 current output
10	VDD	Power	Power supply
11	VSS	Power	Ground
12	I1 out	Output (analog)	Channel 1 current output
13	VDD	Power	Power supply
14	VSS	Power	Ground
15	I0out	Output (analog)	Channel 0 current output
16	VDD	Power	Power supply
17	VSS	Power	Ground
18	VDD	Power	Power supply
19	DRES6	Input	Registers bit 6 value at system reset (internal pull-down)
20	I2CADD6	Input	I2C address bit 6 (internal pull-down)
21	I2CADD5	Input	I2C address bit 5 (internal pull-down)
22	I2CADD4	Input	I2C address bit 4 (internal pull-down)
23	I2CADD3	Input	I2C address bit 3 (internal pull-down)
24	I2CADD2	Input	I2C address bit 2 (internal pull-down)
25	V0-	Input (analog)	Channel 0 voltage input (inverting)
26	V0+	Input (analog)	Channel 0 voltage input (non-inverting)
27	VSS	Power	Ground
28	V1-	Input (analog)	Channel 1 voltage input (inverting)
29	V1+	Input (analog)	Channel 1 voltage input (non-inverting)
30	VDD	Power	Power supply
31	V2-	Input (analog)	Channel 2 voltage input (inverting)
32	V2+	Input (analog)	Channel 2 voltage input (non-inverting)

References

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Document History

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| Rev. 4.0 (June 2001) | Draft manual for the new Laser Driver v2 (LLD2). |
| Rev. 4.1 (January 2002) | Minor corrections (pp.8-9). |

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Appendix A: Changes from previous version

FUNCTIONALITY

- (1) Modularity decreased to 3 channels per chip.
- (2) A choice has been done between the two modes of operation (sink and source) of the previous version. Only the sink mode has been kept.
- (3) The pre-bias current range has been scaled from 5/55mA to 0/55mA.

PROBLEMS SOLVED

- (1) Problems with the I2C logic: the generation of the acknowledge during the read cycle has been fixed.
- (2) A Schmidt Trigger has been added to the following inputs: SDA, SCL, RESb. The serial interface is now suited to work with a larger variety of master characteristics.
- (3) The sequence of data bits during a transfer has been inverted in order to be fully compatible with the standard I2C protocol.
- (4) ESD protection diodes have been added also to output and bi-directional IO pads. All IO pads (both analogue and digital) are now ESD protected.
- (5) The output stages of the linear-drivers have independent un-decoupled power supplies. This scheme has proven in simulation to give a superior noise-immunity performance.
- (6) Four dynamically triggered power clamps have been added to the main power supply to protect the circuit from power spikes.
- (7) Diode strings (5 series diodes, plus one snubber diode) have been added to connect the three output-stage power supplies to the main power supply. The overall ESD scheme provides current paths between every pin combination. At the same time, the usage of several diodes in series keeps a low capacitive coupling between the different supplies.
- (8) The SDA output stage is slew-rate controlled and adaptative (~3ns rise/fall into 10pF).
- (9) Based on simulation, the frequency response of the linear-driver has been improved, without impairing noise, CMRR or PSRR. This has been achieved by equalising the frequency response of the different signal paths and by adding small compensation capacitors.