Radiation Tolerant Linear Laser Driver IC

Reference and Technical Manual

G. Cervelli(*), P. Moreira, A. Marchioro and F. Vasey

CERN, EP Division, CH 1211 Geneva 23, Switzerland

January 2001

Version 2.2

(*) giovanni.cervelli@cern.ch

Introduction

A new version of the four-channel Linear Laser-Driver IC has been designed by the CERN EP Microelectronics group, and implemented in a radiation tolerant CMOS technology. The IC is targeted for the transmission of analogue data from the CMS central tracker detectors (silicon microstrip) to the front-end digitiser cards. The ASIC drives a group of four laser-diodes converting the analogue data produced by the front-end APV chips into amplitude modulated optical signals. Each laser-driver in the IC contains a programmable current source allowing independent biasing of any of the four laser-diodes in its linear region of operation. The same component is well suited to drive the less demanding digital optical links, for TTC signal distribution.

This document is intended to provide a functional and physical description of the Linear Laser-Driver IC.

CMS TRACKER READ-OUT ARCHITECTURE OVERVIEW

The CMS Tracker read-out architecture is described in [1], [2] and [3]. In order to put the Linear Laser-Driver IC into context, we present in this introduction an overview of the CMS tracker read-out architecture. The description done here is brief, simplified and it does not pretend to represent accurately the final system implementation.

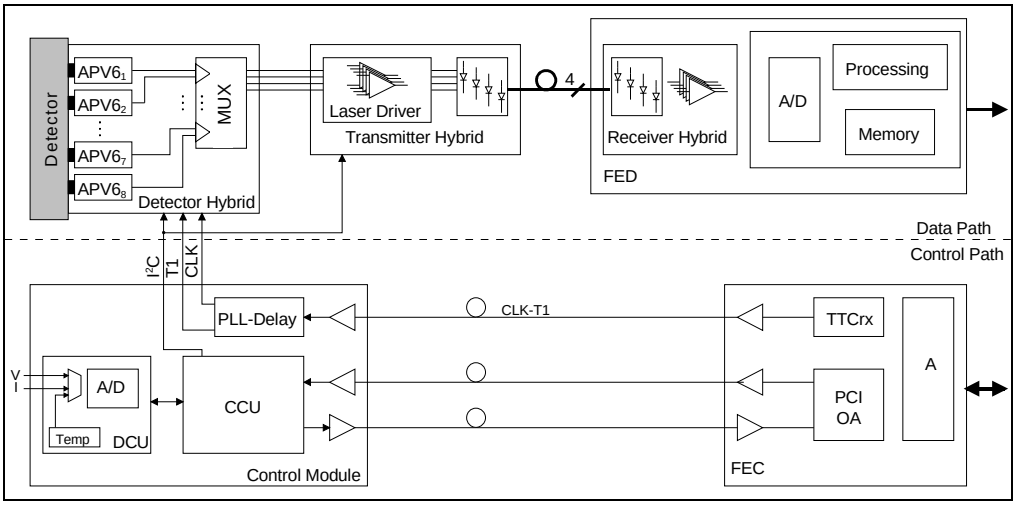


Figure 1 General tracker read-out architecture

Figure 1 represents the general read-out architecture that will serve the CMS tracker. On the occurrence of a first level trigger, the analogue signals that have been previously processed and pipelined by eight APV front-end ICs are sent to the transmitter hybrid by passing through the external multiplexer IC (MUX in Figure 1). The main function of this IC is to time division multiplex the analogue data from eight APVs into four communication channels. Since the data rate at the output of each APV is 20 Mbaud, each communication channel carries a 40 Mbaud data stream. Communication between the two hybrids is made using short lengths of twisted pair copper cables (0-30 cm) of 100 Ω characteristic impedance. In the transmitter hybrids, the Linear Laser-Driver IC and the laser-diodes convert the electrical signals

into optical signals. No special modulation scheme is used and the analogue data is transmitted as amplitude modulated optical signal. Optical fibres are used to send the data to the Front-End Digitiser (FED) modules outside the detectors. Since each APV IC serves 128 detector channels, a single optical fibre link is used to transmit data from 256 channels. In the system there will be approximately a total number of 12 million detector channels (Si-strips) corresponding to 50 thousand optical read-out links.

Laser-Driver IC Specifications

The data transferred from the detector to the FED modules is in the form of pulse amplitude modulated analogue signal. In order to achieve the required system signal-to-noise ratio the electrical-to-optical conversion has to be made with minimum noise and non-linear distortion. An objective for the whole communication channel – from the APVs outputs to the digitising modules – is to achieve a performance equivalent to that of a 7-bit digital system. Each link element should thus exceed this performance. The goal fixed for the Linear Laser-Driver IC was to attain an 8-bit equivalent performance. Taking into account this requirement and the modularity of the data path, the following specifications were set [4] [5]:

- Technology: 0.25 µm CMOS (using radiation tolerant layout technique [6] [7])
- Modularity: Four channels per IC
- Input impedance: 100 Ω (to be set by external resistor)
- Input signal: ±300 mV differential (for specified linearity)
±400 mV differential (maximum)
±250 mV common mode range
- Trans-conductance: 5 / 7.5 / 10 / 12.5 mS (pre-settable)
- Pre-bias current: 5-60 mA (bipolar)
- Dynamic range: 8 bits (50 dB)
- Linear deviation: < 1% (over the operation range)
- Equivalent input noise: < 0.8 mV
- Bandwidth: > 100 MHz
- Settling time: < 10 ns to within 1% of the final value
- Cross-talk: < -60 dB
- Delay uniformity: < 1 ns
- Power supply: ±1.25 V (±10%)
- Power dissipation/channel: 30 mW (minimum pre-bias current)
200 mW (maximum pre-bias current)
- Other: I2C interface (SEU robust)
Individual programming of each channel
Individual per channel power-down function
Start-up mode for digital link

The Linear Laser-Driver IC

In this chapter the Linear Laser-Driver IC architecture, functionality, circuits and physical implementation are described.

ARCHITECTURE

The block diagram of the Linear Laser-Driver IC is represented in Figure 2. The IC is made of four Laser-Drivers (LD) and of an I^2C interface. Each driver takes a differential input voltage and converts it into an unipolar current that is used to modulate an external laser-diode. The analogue input signal is transmitted to the IC using a 100 Ω twisted pair cable. To avoid reflections of the signal — and consequently bad settling times — it is important to terminate the cable in its characteristic impedance. Since, in the IC technology used, there where no precision resistors available, it is necessary to terminate the cable using an external 100 Ω precision resistor as close as possible to the IC.

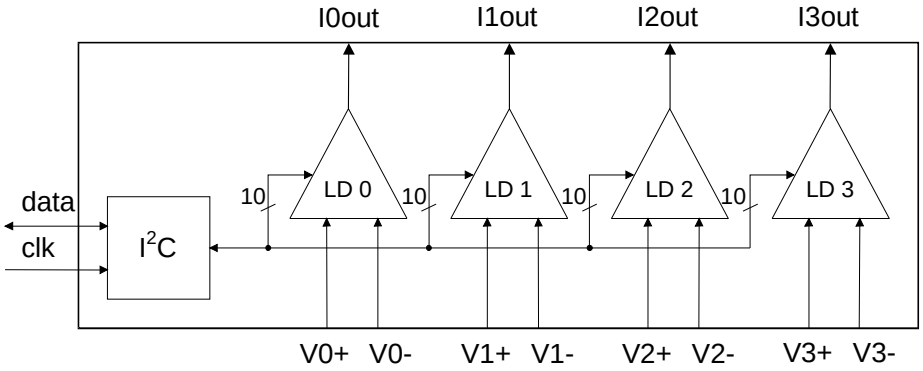


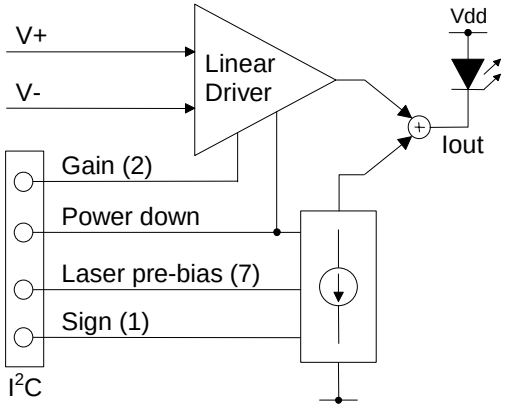
Figure 2 Linear Laser-Driver IC block diagram

Besides signal modulation each driver also generates a *dc* current that is used to bias the external laser-diode. This current allows the laser-diode to be operated above threshold in the linear region of its characteristics. As shown in Figure 3 the modulation current and the bias current are independently processed and summed in the output node. Device ageing and performance degradation due to radiation cause the laser-diodes threshold currents to change with time. To compensate for these variations the laser-diode bias current was made programmable trough the I^2C interface. Since each device in the group will have different thresholds and might age differently, the bias current produced by each driver was made individually programmable.

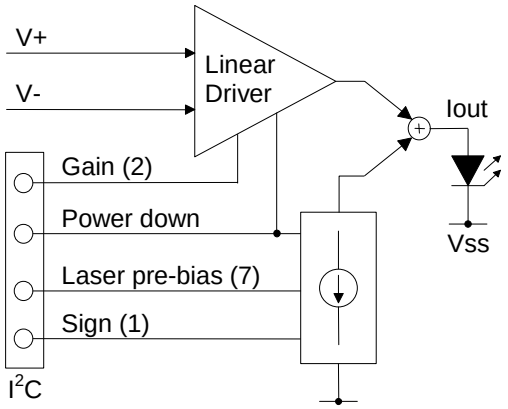
Monolithic arrays of laser diodes are also being considered as candidate devices to be used inside the tracker. They are normally manufactured as either common-cathode or common-anode arrays. Therefore, the Laser Driver IC must be able to either source the dc-current (*source-mode* of operation) or sink it (*sink-mode* of operation). The *sign* bit (shown in Figure 3) is provided for this purpose. The denomination of non-inverting and inverting inputs is opposite in the two modes of operation (the input that is non-inverting in source-mode becomes inverting in sink-mode and vice-versa). The driver output should be connected to the anode of the

laser diode, when operating in source mode, and to its cathode, when operating in sink mode.

Gain variability and enabling/disabling of individual channels is also provided, and can be controlled by the I2C interface. The driver gain variability allows an optimum equalisation of the analogue transmission chain. The power down function allows reducing the power consumption and noise of non-used or defective channels.



(a)



(b)

Figure 3 Laser-Driver block diagram, and diode connection in the two modes of operation: (a) sink mode, and (b) source mode.

FUNCTIONAL

Laser-Diver

Each Laser-Driver in the IC typically works with an input differential voltage between ±300 mV. Within this range the integral non-linearity of the output current is guarantied to be less than 1%. Each driver can however accept differential input voltages up to ±400 mV. Above this limit, the output current is not specified and can eventually saturate. The driver trans-conductance is pre-settable among four different values (5, 7.5, 10 and 12.5 mS), by acting on the 2 gain bits. This results in an output current range of ±2, ±3, ±4 and ±5 mA respectively, when the input differential voltage changes from –400 mV to +400 mV. The laser-diode bias current is generated inside each Laser-Driver. This current is programmable through the I^2C interface between 5-60 mA in steps of 0.4 mA. (7-bit resolution). The current can be set to be positive or negative (sign bit), to allow IC operation in source-mode or sink-mode respectively.

The IC operates between ±1.25 V power supplies. For this power supply the common mode input range is defined as ±250 mV around 0 V. Within this common mode range the IC behaves according to the specified performance.

I^2C Interface

The Linear Laser-Driver IC implements a standard I^2C protocol [8]. The IC contains six internal 8-bit registers. Four read/write registers are used to independently program the external laser-diodes bias-currents (7-bit module and sign). One read/write register is used to program the gains of the four channels (2-bits per channel). The additional read-only register contains a flag that is activated when an SEU event is detected (SEU flag).

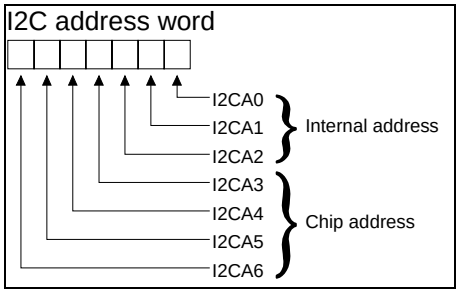


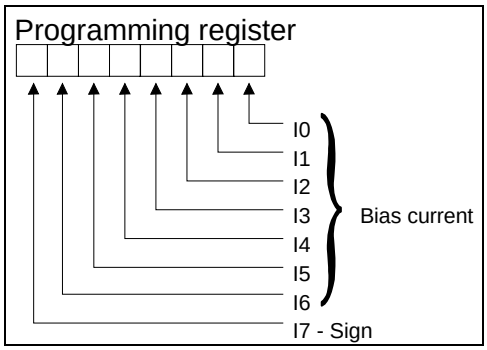
Figure 4 I^2C address decoding

The IC is addressed using a seven bit address number (I2CA6 to I2CA0). Bits I2CA2, I2CA1 and I2CA0 are used to address the six internal programming registers (see Figure 4). Bits I2CA6 to I2CA3 are the IC address, which must be configured using the external ASIC inputs with the same names. It should be noted that those inputs contain internal pull-down resistors. They should be hard-wired to the positive power supply for logical ‘1’ or left open for logical ‘0’. The inputs are not latched by the IC logic and, consequently, they should remain stable during operation.

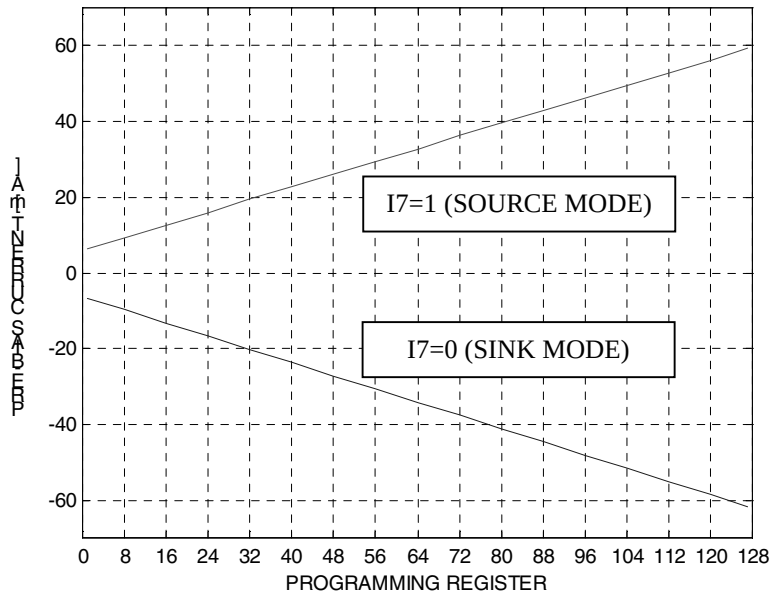
The laser-diodes bias currents are controlled by writing in the four bias-current programming registers. These registers accept the standard 8-bits of data from the I^2C interface (Figure 5). The seven least significant bits control the magnitude of the bias current. This current is approximately given by the programmed number times

0.4 mA in addition to a constant offset of 5 mA. The most significant bit in each register controls the sign of the bias current and thus the mode of operation of each individual channel.

The seven last significant bits also control the power-down function for each individual channel. When the seven least significant bits are simultaneously set to zero, the power-down function is activated. This conventional configuration of bits in a register disables the corresponding driver, thus reducing the power consumption and noise of a non-used or defective channel.



(a)



(b)

Figure 5 Bias-current programming register

The gain programming register (Figure 6) determines the gain of the individual channels. Two bits per channel allow choosing the gain among the four pre-settable values, according to the following table

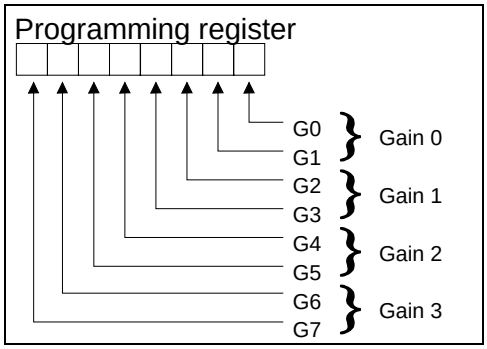


Figure 6 Gain programming register

Gain bit-1	Gain bit-0	Gain value
'0'	'0'	5.0 mS
'0'	'1'	7.5 mS
'1'	'0'	10.0 mS
'1'	'1'	12.5 mS

Table 1 Gain values

The Laser Driver IC is intended to operate in a harsh radiation environment, and it is therefore susceptible to Single Event Upsets (SEU) which could eventually upset the contents of the I2C interface registers. The interface robustness to SEU is increased by tripling all the logic and all the registers, and by using a majority voting decision scheme. This means that the content of the registers is actually stored in three memory locations, which are constantly compared bit by bit. The value which is actually passed through (and which determines the behaviour of the analogue blocks) is the one which is stored in at least two of the three memory locations. As an additional precaution, the event of one memory location being corrupted in any of the register triples is detected and flagged in the status register (see Figure 7). The least significant bit (SEU flag) of the status register indicates if such an event has occurred ('1') or not ('0'). The strategy for scanning the SEU flag and eventually reprogramming the registers is to be defined by the user.

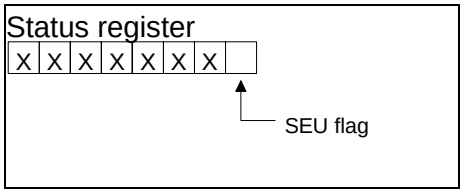


Figure 7 Status register (read-only)

Reset Logic

The Laser Driver IC contains two reset inputs: the power-on reset input (PONb) and the system reset input (RESb). Both of them work on a negative logic (b=bar). The PONb input must be connected to an external RC network (as shown in Figure 8). The time constant τ=1/RC must be greater than the switching-on time of the power supply.

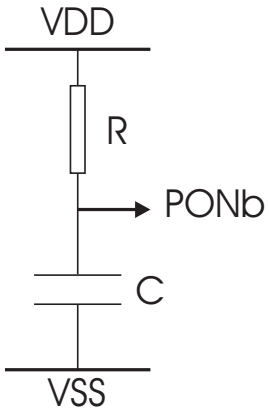


Figure 8 Power-on reset network

The system reset input can be optionally connected to a remote control. An internal pull-up resistor insures that RESb stays high in case it is not connected.

On occurrence of a reset (power-on or system reset), all the registers are set to their initial values. The initial value of the bias-current programming registers can be pre-set by connecting the inputs DRES4, DRES5, DRES6 and DRES7. These inputs are common to the four driver channels and determine the initial value of the 4 most significant bits of the programming registers (I4 to I7). The 4 least significant bits are reset to logical ‘0’s. It should be noted that these inputs contain internal pull-down resistors. Thus it is necessary to hard-wire them to positive power supply to program a logical ‘1’, while they can be left open to program a logical ‘0’. For the more numerous analogue links, it is convenient that the drivers stay disabled when the system is powered or reset, until the first I2C write operation. Therefore, the DRES inputs must simply be left unconnected. For the digital links, however, the lasers *must* be active at system start-up or reset, to insure the possibility of communication between the detector front-ends and the outside world. In this case, the initial bias-current of the lasers must be configured using the DRES inputs. The gain programming register is in all cases reset to all ‘1’s.

LASER-DRIVER CIRCUITS

IC Bias

A simplified schematic of the IC bias circuit is represented in Figure 9. This consist of a standard *bootstrap reference* [9], where the reference current I_{ref} is approximately given by V_{T1}/R and the corresponding reference voltage V_{ref} is used to bias the IC. The left-hand part of the circuit (dotted) insures that the circuit is correctly bootstrapped, but is cut-off during normal operation. This circuit technique can be implemented in a full CMOS technology and has the advantage of being relatively immune to power-supply noise.

To minimise cross talk among the different channels each driver in the IC contains its own bias circuit. This results in an increase of the ASIC power consumption. However, the incurred power penalty is small since the bias circuit contributes only with a small fraction to the total power consumption.

A power-down function is also implemented in this circuit by the switches shown in Figure 9. Since the driver works by duplication and multiplication of the reference current, once this current is forced to zero no power is available to the driver circuits reducing the power consumption essentially to zero. The power-down function is controlled by the I^2C interface as explained in the previous section (see I^2C Interface).

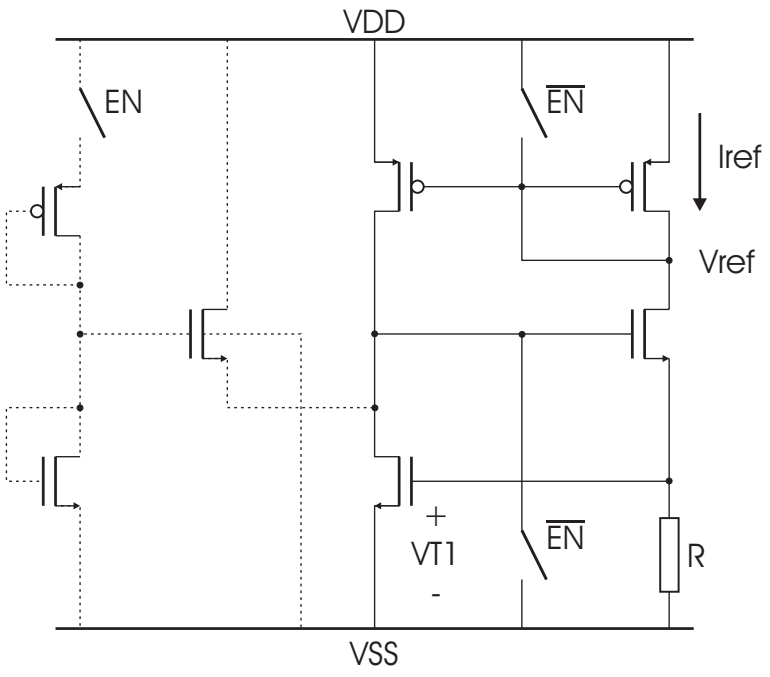


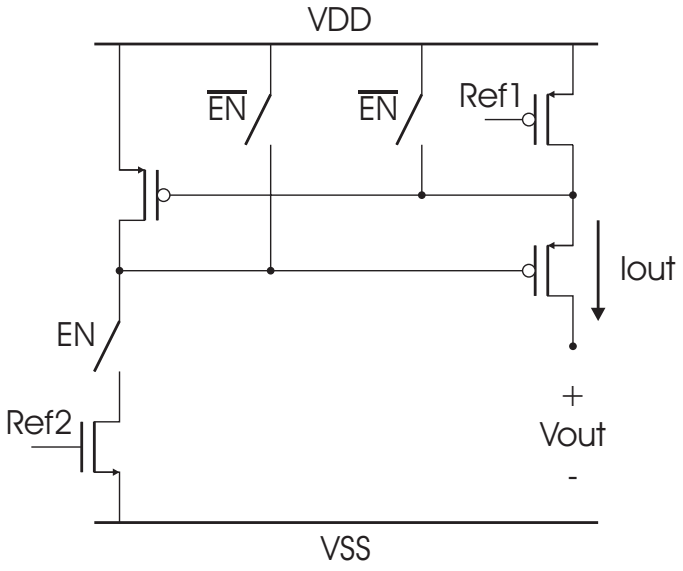
Figure 9 Bootstrap current reference

Laser-Diode Bias Circuit

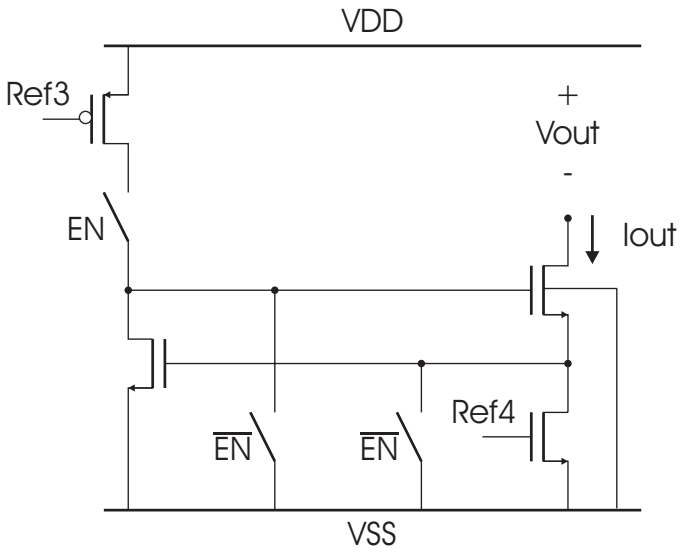
The laser-diode bias circuit consists of an array of 282 elementary sources (Figure 10a) and sinks (Figure 10b). As mentioned before, this circuit allows to bias the laser-diode in its linear region of operation and to compensate for device-to-device variations, device ageing and device performance degradation due to radiation. The elementary sources or sinks are switched-on and off, according to the contents of the

programming registers. A positive or negative current can be programmed whose module is linearly variable between 5 mA and 60 mA. The current range between –5 mA and +5 mA is not covered, since it corresponds to under-threshold operation for all lasers being considered.

The elementary sources / sinks have been implemented using the regulated-cascode technique [10]. This scheme has the advantage of providing relatively high output impedance, while the compliance output voltage and the power-supply rejection-ratio are still compatible with the specification. The reference voltages *Ref1*, *Ref2*, *Ref3* and *Ref4* are generated by two independent reference circuits of the kind described in the previous section (see IC Bias).



(a)



(b)

Figure 10 Laser-diode bias circuit

Linear-Driver

The Linear-Driver is the part of the Laser-Driver that is responsible for signal modulation of the laser-diode. This is the only part of the circuit with currents actually switching during normal operation[1].

A simplified schematic of the Linear-Driver is shown in Figure 11. The Linear-Driver consists of a differential-pair preamplifier (left-hand side of the schematic) and a push-pull output stage (right-hand side of the schematic). The differential-pair amplifies the input differential voltage and converts it in a differential current, which is amplified and summed by the output stage. The differential-pair, compared with alternative design solutions, is conceptually simple and offers good dynamic and noise performance at limited power dissipation. The PMOS version is bulk-effect-free, thus allowing a larger input common-mode range. The push-pull output stage is symmetrical and is thus compatible with the two modes of operation (source mode and sink mode).

The output stage actually consists of three stages in parallel, with binary weighed gain and current summation at the output. The first stage (gain = 2) is always active, whereas the second and third stages (gain = 1 and 2) can be switched on and off, according to the contents of the gain programming register. The overall gain of the output stage can be 2, 3, 4 or 5. This has to be multiplied with the gain of the differential-pair pre-amplifier of 2.5 mS.

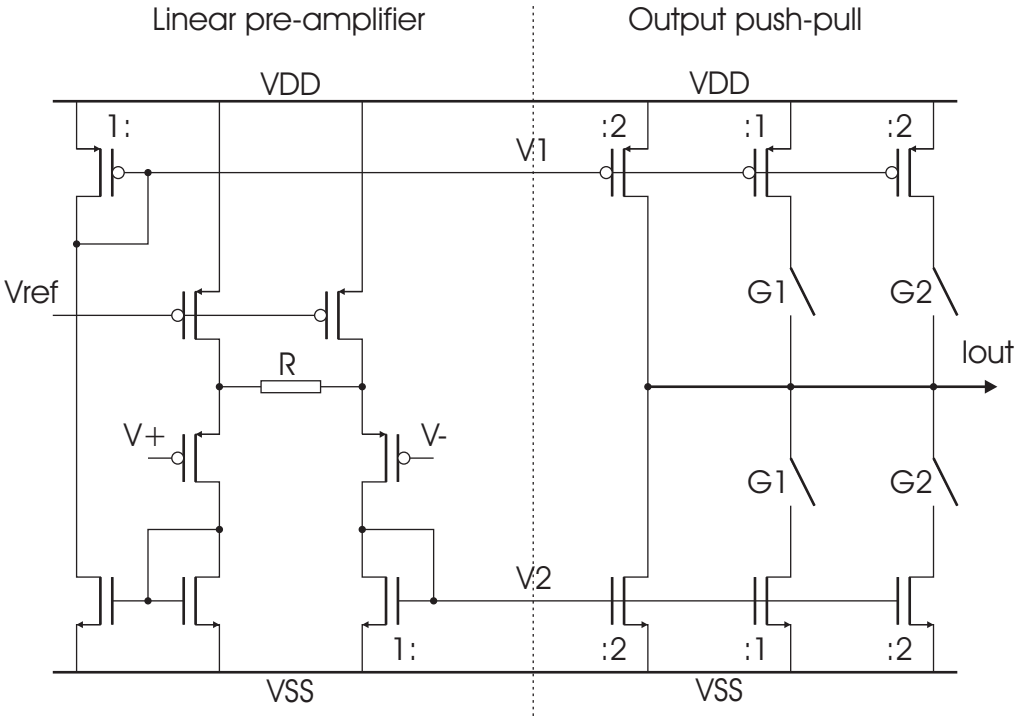
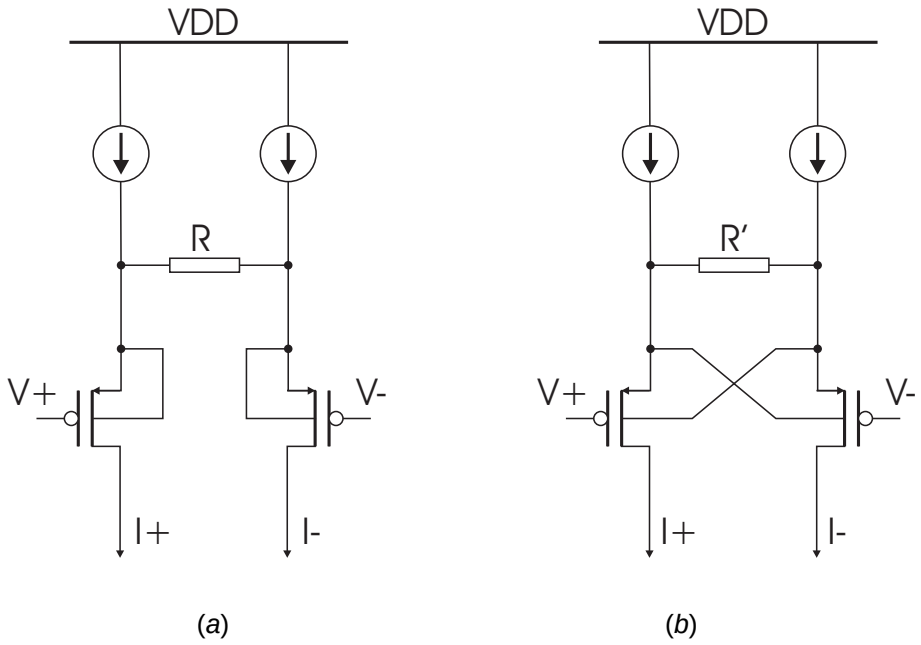


Figure 11 Linear-Driver

The overall current absorbed by the circuit is kept constant (i.e. independent from the input signal), in order to limit as much as possible current fluctuations and noise induced in the power-supplies. The power dissipation of the Linear-Driver is below 30 mW per channel.

[1] The digital logic is quiet during data acquisition. The noise interference should be kept to a minimum during this operation period.

The required linearity is obtained with a combination of two source-degeneration methods: a parallel source-degeneration resistor, and a source-bulk cross-connection between the transistors of the differential-pair (as highlighted in Figure 12). The combination of these two methods allows keeping the degeneration resistor to a value compatible with the required input common-mode range. Source-degeneration methods apply local feedback to achieve the required linearity. Although global feedback can be a more efficient means of linearisation it is also potentially more susceptible to produce stability problems due to output loading effects. Additionally, global feedback is difficult to apply to a differential structure such as the one used. For these reasons, local linearisation was preferred in the design of the Linear-Driver.



(*a*) (*b*)

Figure 12 PMOS differential pair input stage, with parallel source degeneration resistor (*a* and *b*) and with cross-connected sources and bulks (*b* only).

As discussed before input termination has to be made externally to the circuit by means of an 100 Ω resistor as close as possible to the IC. Good input matching is important to avoid the degradation of the input signal settling time due to input signal reflections.

PHYSICAL IMPLEMENTATION

The Linear Laser-Driver IC was fabricated in a standard commercial 0.25µm CMOS process. Figure 13 shows the ASIC foot print. Its dimensions are 2.00 mm × 3.75 mm. The IC has not been packaged for two main reasons: firstly, when in use, the IC will be directly bonded to the transmitter hybrid and secondly, the presence of package inductance is detrimental to the circuit performance.

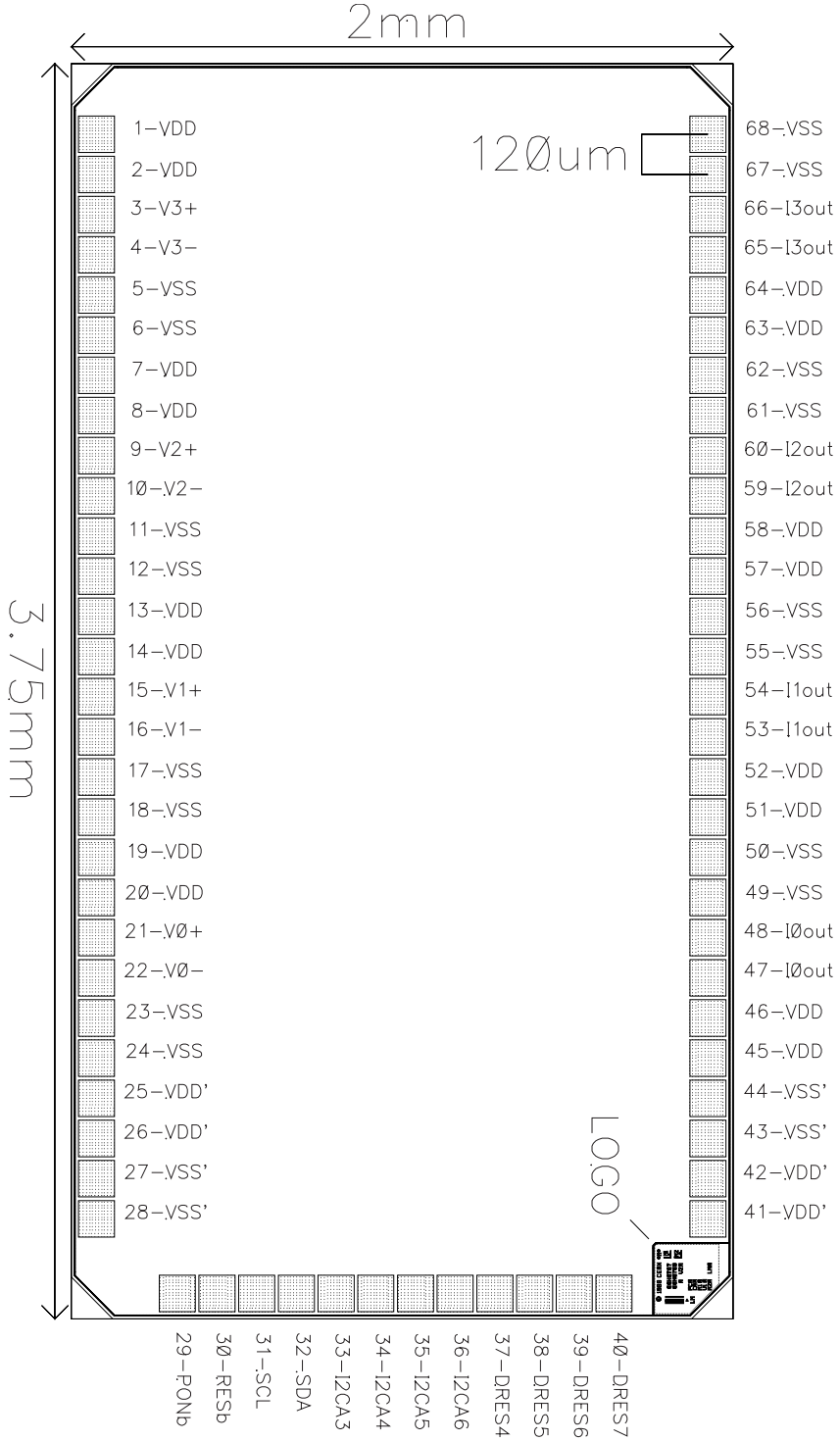


Figure 13 Linear Laser-Driver IC footprint (**Warning!** Note channels renumbering!).

In order to optimise the parasitic inductance and simplify the bonding procedure, most of the analogue IC pads (outputs and power supplies) have been doubled. All the IC pads that have the same name in Figure 13 are internally connected inside the chip. The IC pad pairs can be bonded to the same pad on the hybrid, which is normally bigger. This procedure should allow: (1) to have much less pads on the hybrid then on the chip itself; (2) to reduce the parasitic self inductance due to double (or multiple) bonding; (3) to keep the bonding wires as parallel as possible, thus minimising the wire length and profiting of the mutual inductance cancellation. The proposed bonding diagram is shown in Figure 14.

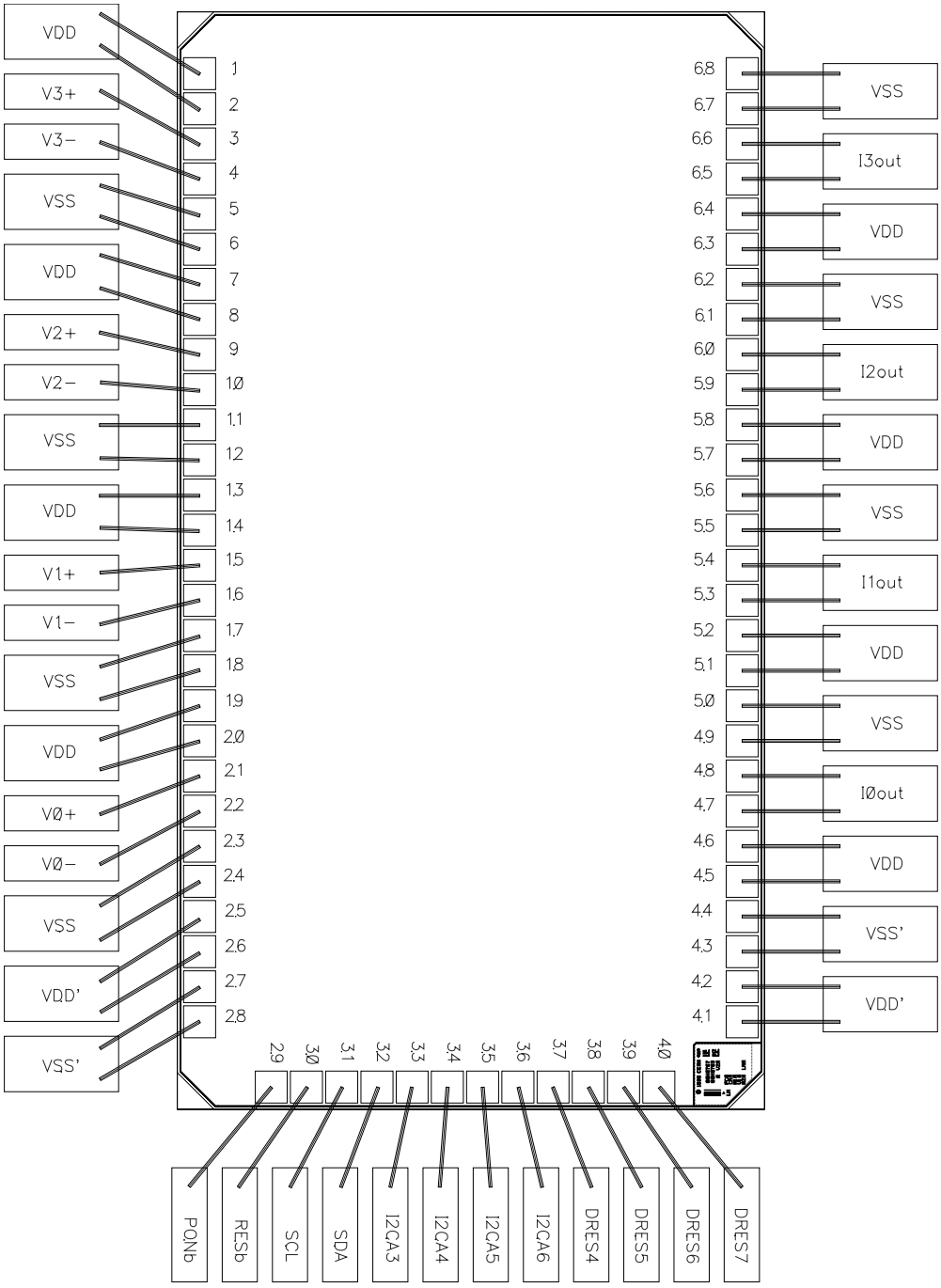


Figure 14 Linear Laser-Driver bonding diagram (**Warning!** Note channels renumbering!).

IC Signals

Warning! Channels have been renumbered in order to be coherent with the I2C internal addressing scheme!

VDD (1, 2, 7, 8, 13, 14, 19, 20, 45, 46, 51, 52, 57, 58, 63, 64)
Positive power supply: +1.25 V

VSS (5, 6, 11, 12, 17, 18, 23, 24, 49, 50, 55, 56, 61, 62, 67, 68)
Negative power supply: -1.25 V

VDD' (25, 26, 41, 42)
Positive power supply: +1.25 V (for digital interface only)

VSS' (27, 28, 43, 44)
Negative power supply: -1.25 V (for digital interface only)

V3+ (3)	Channel 0 voltage input '+' (*)
V3- (4)	Channel 0 voltage input '-' (**)
V2+ (9)	Channel 1 voltage input '+' (*)
V2- (10)	Channel 1 voltage input '-' (**)
V1+ (15)	Channel 2 voltage input '+' (*)
V1- (16)	Channel 2 voltage input '-' (**)
V0+ (21)	Channel 3 voltage input '+' (*)
V0- (22)	Channel 3 voltage input '-' (**)
I3out (65, 66)	Channel 0 current output
I2out (59, 60)	Channel 1 current output
I1out (53, 54)	Channel 2 current output
I0out (47, 48)	Channel 3 current output
PONb (29)	Power-on reset (to be connected to external RC network)
RESb (30)	System reset (internal pull-up)
SCL (31)	I^2C system clock input (to be connected to external pull-up)
SDA (32)	I^2C serial data input / output (to be connected to external pull-up)
I2CA3 (33)	I^2C address bit number 3 (internal pull-down)
I2CA4 (34)	I^2C address bit number 4 (internal pull-down)
I2CA5 (35)	I^2C address bit number 5 (internal pull-down)
I2CA6 (36)	I^2C address bit number 6 (internal pull-down)
DRES4 (37)	Registers bit 4 value at system reset (internal pull-down)
DRES5 (38)	Registers bit 5 value at system reset (internal pull-down)
DRES6 (39)	Registers bit 6 value at system reset (internal pull-down)
DRES7 (40)	Registers bit 7 value at system reset (internal pull-down)

(*) Input '+' is inverting in source-mode and non-inverting in sink-mode.

(**) Input '-' is non-inverting in source-mode and inverting in sink-mode.

References

[1] CMS Collaboration, The Compact Muon Solenoid, Technical Proposal, CERN/LHCC/94-38, 1994.

[2] CMS WWW Welcome page (http://cmsinfo.cern.ch/Welcome.html).

[3] CMS Collaboration, The Tracker Project, Technical Design Report, CERN/LHCC/98-6, 1998.

[4] A. Marchioro, P. Moreira, T. Toifl and T. Vaaraniemi, An integrated laser driver array for analogue data transmission in the LHC experiments, Proceedings of the Third workshop on electronics for LHC experiments, CERN/LHCC/97-60, London, 1997, pp. 282-286.

[5] P. Moreira, A. Marchioro, Linear Laser Driver IC – reference and technical manual, Version 1.1, CERN / EP / MIC, December 1997.

[6] A. Rivetti, G. Anelli, F. Anghinolfi et al., Analog Design in Deep Sub-micron CMOS Processes for LHC, Proceedings of the Fifth workshop on electronics for LHC experiments, CERN/LHCC/99-33, Snowmass, 1999, pp. 157-161.

[7] P. Jarron, G. Anelli, T. Calin et al., Deep sub-micron CMOS technologies for the LHC experiments, Nuclear Physics B (Proceedings Supplements), Vol. 78, 1999, pp. 625-634.

[8] I^2C bus specifications, Philips Semiconductors, January 2000 (http://www-eu3.semiconductors.com/i2c/).

[9] P. Allen, D. Holberg, CMOS Analog Circuit Design, Saunders College Publishing, 1987.

[10] E. Säckinger, W. Guggenbühl, A high-swing high-impedance MOS cascode circuit, IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, February 1990.

Document History

Rev. 2.0 (August 2000)	Draft.
Rev. 2.1 (November 2000)	Rework. Parts added.
Rev. 2.2 (January 2001)	Channel numbering corrected. Added Appendix A.

Contact Persons

Giovanni Cervelli

CERN, EP Division, CH 1211 Geneva 23

E.mail: giovanni.cervelli@cern.ch

Phone: +41-22-7677336

Appendix A: Known Problems

PROBLEMS WITH I2C INTERFACE

(1) The present version of the I2C interface has a problem in *acknowledging a read cycle when a '1' is present in the least significant bit (LSB) of the register*. It is therefore not possible to read the content of a register when its LSB is at '1'. It is however possible to *write* correctly any configuration in any register and therefore to access the full functionality of the device.

(2) The I2C interface inputs show a strong sensitivity to slowly rising/falling signals (eventually causing glitches in the logical inputs, which might be wrongly interpreted as logical transitions). This problem is being investigated.

(3) The address bits are flipped inside the I2C interface. Thus when writing an address to the I2C interface, the bits should be sent sequentially starting with the LSB to the MSB. This is inverted in relation with the standard I2C protocol.