

Linear Laser-Driver IC

Reference and Technical Manual

P. Moreira^{*} and A. Marchioro[†]

CERN-ECP/MIC, Geneva Switzerland

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^{*} E-mail: Paulo.Moreira@cern.ch

[†] E-mail: Alessandro.Marchioro@cern.ch

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Introduction

A four-channel Linear Laser-Driver IC has been designed by the CERN ECP Microelectronics group. The IC is used for the transmission of analogue data from the CMS central tracker detectors — gas and silicon microstrip — to the front-end digitiser cards. The ASIC drives an array of four laser-diodes converting the analogue data produced by the front-end APV chips into amplitude modulated optical signals. Each laser-driver in the IC contains a programmable current source allowing independent biasing of any of the four laser-diodes in its linear region of operation.

This document is intended to provide a functional and physical description of the Linear Laser-Driver IC.

CMS TRACKER READ-OUT ARCHITECTURE OVERVIEW

The CMS Tracker read-out architecture is still under development [1] and [2]. However, the specification of the data path between the APV front-end ICs and the digitising cards is now at a level of detail that allows the development and prototyping of the data link basic components. In order to put the Linear Laser-Driver IC into context, we present in this introduction an overview of the CMS tracker read-out architecture. The description done here is brief, simplified and it does not pretend to represent accurately the final system implementation. Detailed information about the general read-out architecture, the current developments and the system specifications can be found in references [1] to [8].

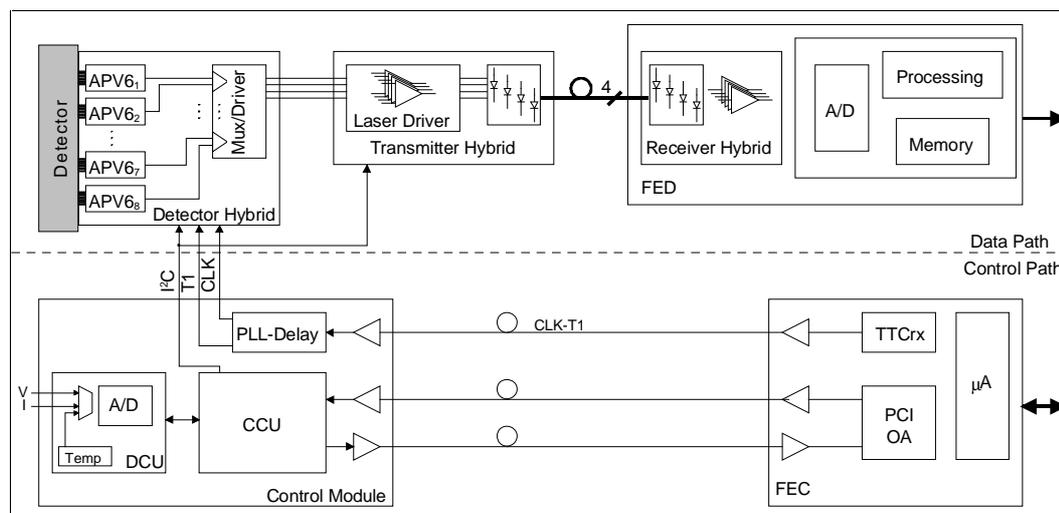


Figure 1 General tracker read-out architecture

The CMS tracker consists of two detectors: an inner cylinder of silicon microstrip (Si-strips) detectors and an outer layer of gas micro-strip chambers (MSGCs) [1]. Figure 1 represents the general read-out architecture that will serve both types of detectors. On the occurrence of a first level trigger, the analogue signals that have been previously processed and pipelined by eight APV front-end ICs are sent to the transmitter hybrid by the APV-Mux ASIC (Mux/Driver in Figure 1). The main function of this IC is to time division multiplex the analogue data from eight APVs into four communication channels. Since the data rate at the output of each APV is 20 Mbaud, each communication channel carries a 40 Mbaud data stream. Besides data multiplexing the APV-Mux converts the current output of the eight APVs into a voltage output, provides signal amplification and driving capability to transmit the data from

the detector hybrids to the transmitter hybrids. Communication between the two hybrids is made using short lengths of twisted pair copper cables (0-30 cm) of 100 Ω characteristic impedance. In the transmitter hybrids the electrical signals are converted into optical signals by the Linear Laser-Driver IC and the laser-diodes. No special modulation scheme is used and the analogue data is transmitted as an amplitude modulated optical signal. Optical fibres are used to send the data to the Front End Digitiser (FED) modules outside the detectors. Since each APV IC serves 128 detector channels, a single optical fibre link is used to transmit data from 256 channels. In the system there will be approximately a total number of 12 million detector channels (Si-strips and MSGCs) corresponding to a total of 50 thousand optical read-out links.

Laser-Driver IC Specifications

The data transferred from the detector to the FED modules is in the form of an amplitude modulated analogue signal. In order to achieve the required system signal-to-noise ratio the electrical-to-optical conversion has to be made with minimum noise and non-linear distortion. An objective for the whole communication channel – from the APVs outputs to the digitising modules – is to achieve a performance equivalent to that of a 7-bit digital system. Each link element should thus exceed this performance. The goal fixed for the Linear Laser-Driver IC was to attain an 8-bit equivalent performance. Taking into account this requirement and the modularity of the data path the following specifications were set:

◆ Technology:	Radiation hard ¹
◆ Modularity:	Four channels per IC
◆ Input impedance:	100 Ω
◆ Input signal:	± 400 mV differential (for specified linearity)
◆	± 800 mV differential (maximum)
◆	± 250 mV common mode range
◆ Modulation current:	5 mA
◆ Pre-bias current:	0-25 mA
◆ Dynamic range:	8 bits
◆ Linear deviation:	< 1% (over the operation range)
◆ Equivalent input noise:	< 1 mV
◆ Bandwidth:	> 70 MHz
◆ Settling time:	< 10 ns to within 1% of the final value
◆ Crosstalk:	< 0.3%
◆ Delay uniformity:	< 1 ns
◆ Power supply:	± 2 V
◆ Power dissipation/driver:	50 mW (minimum pre-bias current)
◆	150 mW (maximum pre-bias current)
◆ Other:	I2C interface
◆	Individual programming of each channel
◆	Individual per channel power-down function

¹ The Laser Driver IC prototype described in this manual was manufactured in a standard 0.8 μm BiCMOS technology. A future implementation in a radiation hard technology is planned.

The Linear Laser-Driver IC

In this chapter the Linear Laser-Driver IC architecture, functionality, circuits and physical implementation are described.

ARCHITECTURE

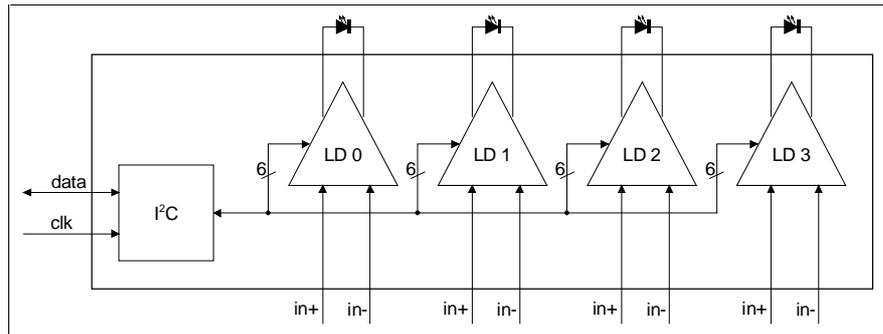


Figure 2 Linear Laser-Driver IC block diagram

The block diagram of the Linear Laser-Driver IC is represented in Figure 2. The IC is made of four Laser-Drivers (LD) and of an I²C interface. Each driver takes a differential input voltage and converts it into an unipolar current that is used to modulate an external laser-diode. Besides signal modulation each driver also generates a *dc* current that is used to bias the external laser-diode. This current allows the laser-diode to be operated above threshold in the linear region of its characteristics. As shown in Figure 3 the modulation current and the bias current are independently processed and summed in the output node.

Device ageing and performance degradation due to radiation cause the laser-diodes threshold currents to change with time. To compensate for these variations the laser-diode bias current was made programmable through the I²C interface. Since each device in the array will have different thresholds and it will age differently, the bias current produced by each driver was made individually programmable.

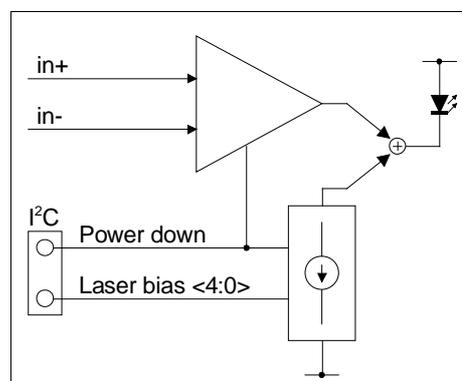


Figure 3 Laser-Driver block diagram

FUNCTIONAL

Laser-Driver

Each Laser-Driver in the IC typically works with an input differential voltage between ± 400 mV. Within this range the integral nonlinearity of the output current is guaranteed to be less than 1%. Each driver can however accept differential input voltages up to ± 800 mV. Above this limit the output current saturates. The driver transconductance is approximately 6.3 mS. This results in an output current change of 5 mA when the input differential voltage changes from -400 mV to +400 mV.

The IC operates between ± 2 V. For this power supply the common mode input range is defined as ± 250 mV around 0 V. Here a more restrictive definition of common mode range is used: this range is defined as being the set of common mode voltages that result in an output current deviation smaller than 1% relative to the output current with 0 V common mode. The common mode range is measured with an input differential voltage of ± 400 mV.

The analogue input signal is transmitted to the IC using a 100 Ω twisted pair cable. To avoid reflections of the signal — and consequently bad settling times — it is important to terminate the cable in its characteristic impedance. Since, in the IC technology used, there where no precision resistors available, it is necessary to terminate the cable using an external 100 Ω precision resistor as close as possible to the IC.

A laser-diode bias current is generated inside each Laser-Driver. This current is programmable through the I²C interface between 0-25 mA in steps of 0.8 mA. It is necessary to note that even when a 0 mA bias current is programmed a non-zero current still flows through the laser-diode. This current is due to the output differential pair tail current and is approximately equal to 4.5 mA when the input differential voltage is 0 V.

I²C Interface

The Linear Laser-Driver IC implements a standard I²C protocol [9]. The IC contains four read/write registers that are used to independently program the external laser-diodes bias currents.

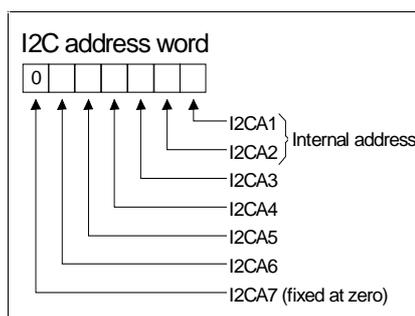


Figure 4 I²C address decoding

The IC is addressed using a seven bit address number (I2CA7 to I2CA1). Bits I2CA2 and I2CA1 are used to address the four internal programming registers (see Figure 4). Bits I2CA6 to I2CA3 are the programmable IC address. These bits are programmed using the external ASIC signals with same names. These signals are not latched by the IC logic and, consequently, they should remain stable during operation. Address bit I2CA7 it is not programmable and is set to zero.

The laser-diodes bias currents are controlled by writing in the four “bias-current programming registers”. These registers accept the standard 8-bits of data from the I²C interface but only the six lower bits are used (Figure 5). The five least significant bits control the bias current. This current is approximately given by the programmed number times 0.8 mA. To obtain the effective quiescent current through the laser-diode it is necessary to add to this number half of the output differential pair tail current which is approximately equal to 4.5 mA.

The bit number six in each register controls the power-down function. For a given register writing a one in this position will disable the corresponding driver. This function allows to reduce the power consumption of a non used or defective channel.

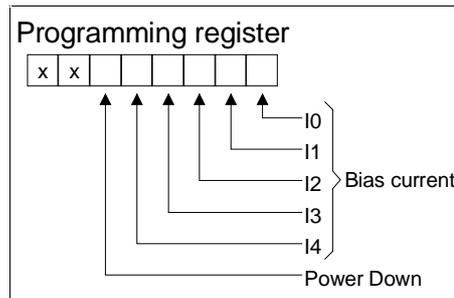


Figure 5 Bias-current programming register

LASER-DRIVER CIRCUITS

IC Bias

To minimise crosstalk among the different channels each driver in the IC contains its own bias circuit. This results in an increase of the ASIC power consumption. However, the incurred power penalty is small since the bias circuit contributes only with a small fraction to the total power consumption.

A simplified schematic of the bias circuit is represented in Figure 6. This reference current generator is composed of a standard bandgap circuit [10] (transistors Q1 Q2, M1 and M2 and resistors R1 and R2) and of a voltage-to-current converter (transistor Q3 and resistor R3). In the voltage-to-current converter, the bandgap voltage at the base of Q1 and Q2 is transformed by R3 into a current with magnitude: $I_{ref} \cong V_{bg} / R3$. Transistor Q3 acts as an emitter follower isolating the collector current of Q2 from the loading effect of R3 and from the base currents of Q1 and Q2.

A power-down function is also implemented in this circuit (details not shown in Figure 6). Since the driver works by duplication and multiplication of the reference current, once this current is forced to zero no power is available to the driver circuits reducing the power consumption essentially to zero. The power-down function is controlled by the I²C interface as explained in the previous section (see I²C Interface).

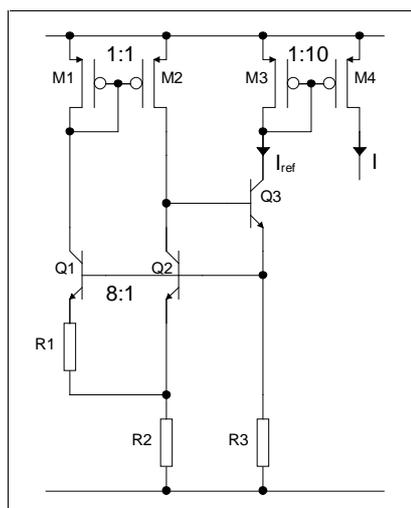


Figure 6 Bandgap current reference

Laser-Diode Bias Circuit

The laser-diode bias circuit, which it is basically a programmable current mirror, it is schematically represented in Figure 7. In this circuit the MOS transistors M1 to M5 make binary weighted copies of the reference current I_{ref} . These current copies are then summed in the base node of the current mirror Q1-Q2. The resulting current is then multiplied by a factor of ten and made available to bias the external laser-diode. To program the current mirror transistors M6 to M10 act as current switches that are controlled by the I²C interface (see I²C Interface). As mentioned before, this circuit allows to bias the laser-diode in its linear region of operation and to compensate for

device-to-device variations, device ageing and device performance degradation due to radiation.

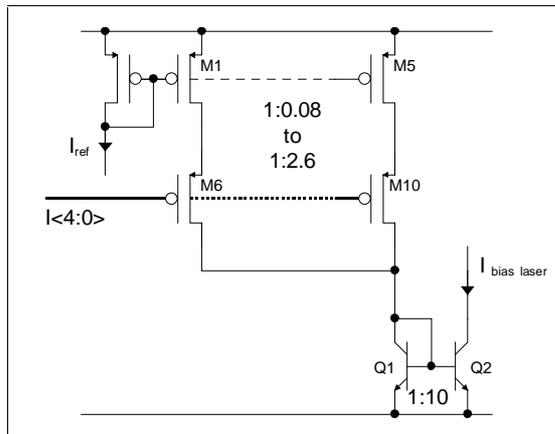


Figure 7 Laser-diode bias circuit

Linear-Driver

The Linear-Driver is the part of the Laser-Driver that is responsible for signal modulation of the laser-diode. This is the only part of the circuit with currents actually switching during normal operation². Since one of the goals of the project was to include four drivers in the same IC, each Linear-Driver was designed as a full differential circuit. In this way, the sensitivity to power supply noise is minimised and the amount of power supply noise generated by each driver is reduced.

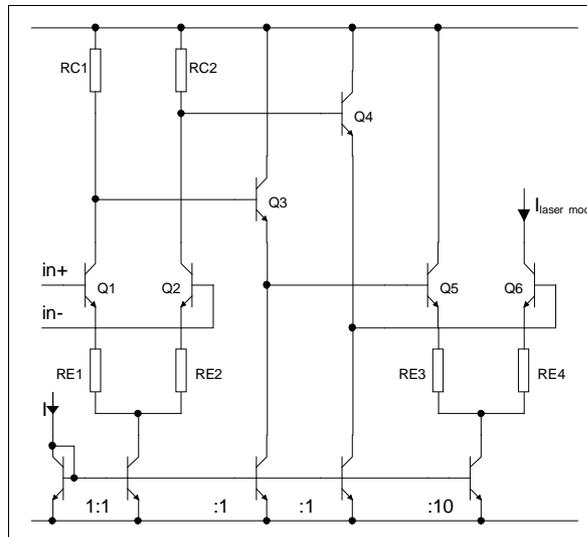


Figure 8 Linear-Driver

As shown in Figure 8 the Linear-Driver contains two differential pairs and a Common-Collector (CC) stage. The first differential pair provides signal gain “adapting” the input signal range to the linear operation range of the output stage. The emitter follower transistors (Q3 and Q4) provide level shifting for correct biasing of the output stage/laser-diode combination. Since all stages – including the CC stages – are

² The digital logic is quiet during data acquisition. This is the operation period during which the noise interference should be kept to a minimum.

biased by constant current sources, the current on both supply rails is – in first order – constant. However, to take advantage of the differential circuit topology to minimise power supply noise coupling a careful layout and power supply strategy for the output stage/laser-diode combination is required. This will be discussed in the next section (see Output Stage Power Supply).

Linearisation of the overall circuit transconductance is made in each differential pair stage by means of local feedback. That is, the overall transconductance is linearised using emitter degeneration resistors (RE1 to RE4) in each one of the differential pairs (see the Appendix for a detailed discussion of the linearisation technique). Since the common-collector stages are biased by a constant current they are intrinsically linear and no special linearisation technique is required in these stages. Although global feedback can be a more efficient means of linearisation of the overall transconductance it is also potentially more susceptible to produce stability problems due to output loading effects. Additionally, global feedback is difficult to apply to a fully differential structure such as the one used. For these reasons local linearisation of the transconductance of each amplifying stage in the Linear-Driver was preferred in this design.

As discussed before input termination has to be made externally to the circuit by means of an $100\ \Omega$ resistor as close as possible to the IC. Good input matching is important to avoid the degradation of the input signal settling time due to input signal reflections.

PHYSICAL IMPLEMENTATION

The Linear Laser-Driver IC was fabricated in a standard commercial 0.8 μ m BiCMOS process. Figure 9 shows the ASIC foot print. Its dimensions are 1.9 mm \times 2.9 mm. The IC has not been packaged for two main reasons: firstly, when in use, the IC will be directly bonded to the transmitter hybrid and secondly, the presence of package inductance is detrimental to the circuit performance.

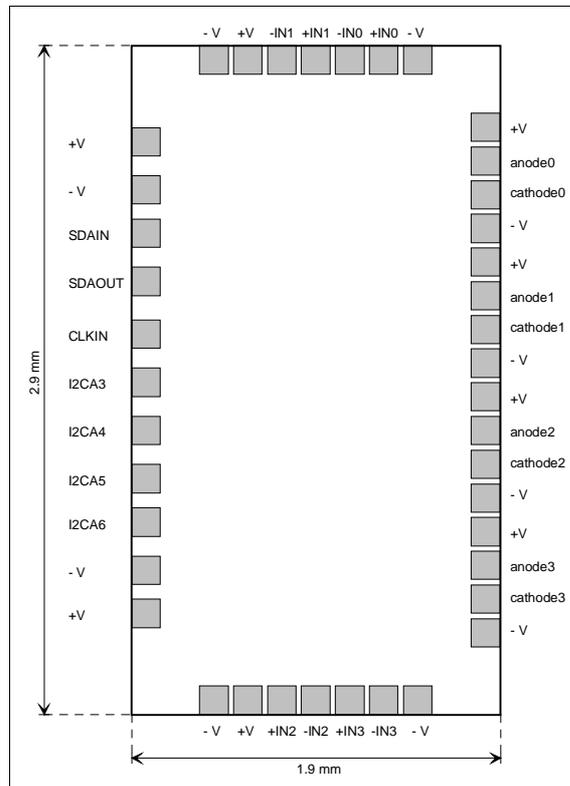


Figure 9 Linear Laser-Driver IC footprint

IC Signals:

- +IN0** – channel 0 non-inverting input
- +IN1** – channel 1 non-inverting input
- +IN2** – channel 2 non-inverting input
- +IN3** – channel 3 non-inverting input
- +V** – positive power supply: +2 V
- IN0** – channel 0 inverting input
- IN1** – channel 1 inverting input
- IN2** – channel 2 inverting input
- IN3** – channel 3 inverting input
- V** – negative power supply: -2 V
- anode0** – channel 0 laser-diode anode connection

- anode1** – channel 1 laser-diode anode connection
- anode2** – channel 2 laser-diode anode connection
- anode3** – channel 3 laser-diode anode connection
- cathode0** – channel 0 laser-diode cathode connection
- cathode1** – channel 1 laser-diode cathode connection
- cathode2** – channel 2 laser-diode cathode connection
- cathode3** – channel 3 laser-diode cathode connection
- CLKIN** – I²C clock input
- I2CA3** – I²C address bit number 3
- I2CA4** – I²C address bit number 4
- I2CA5** – I²C address bit number 5
- I2CA6** – I²C address bit number 6
- SDAIN** – I²C data input (to be connected to the same node as SDAOUT)
- SDAOUT** – I²C data output (to be connected to the same node as SDAIN)

Output Stage Power Supply

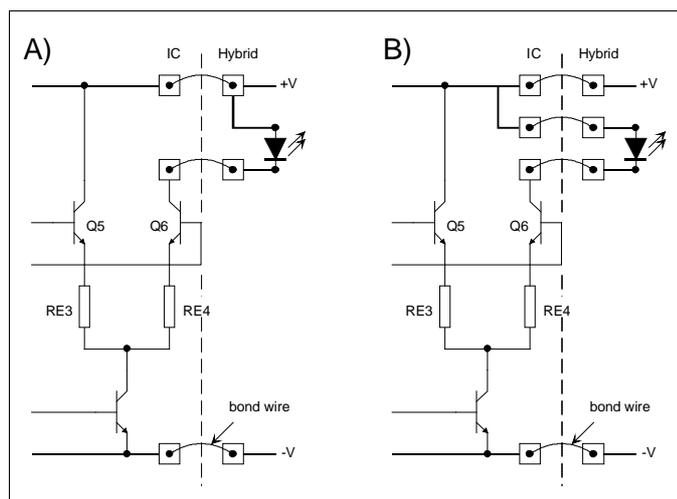


Figure 10 Output stage/laser-diode power supply options

Figure 10 shows two of the possible options that can be used to connect the output stage and the laser-diode to the positive power supply rail (+V). In option A) the bond wire that connects the IC to +V carries the collector current of Q5³. This current changes with time and induces power supply noise in the IC +V rail due to the finite inductance of the bond wire. The amplitude of the induced noise can be important since the output stage is fast enough to switch up to 5 mA in 1 ns. Noise in the +V supply rail can be quite detrimental to the circuit operation because it can couple to the output signal through to mechanisms: In one mechanism the power supply noise modulates the driver bias current which in turn modulates the output differential pair tail current. This tail current modulation passes directly to the output as an unwanted signal. In the other, the noisy bias current is multiplied by the programmable current

³ This bond wire also carries the current to the other parts of the laser-driver circuit. However, this current is constant for all practical purposes. It is does not necessary to consider it in this discussion.

mirror of the Laser-Diode Bias Circuit also resulting in unwanted modulation of the laser-diode. This effect increases for high laser-diode bias currents since in this case high current mirror gains are used. In the second power supply option – Figure 10 B) – the bond wire connecting the IC to the power supply carries the current of both branches of the output differential pair. Since the current variations in both branches are equal in magnitude and have opposite signs they cancel out and the current through bond wire remains constant. In practice this current is not exactly constant due to the presence of the laser-diode impedance in one of the branches. However, simulations show that it is possible, by using this topology, to reduce substantially the +V rail self induced noise. Configuration of Figure 10 B) was the one chosen in this design. This configuration has however the disadvantage of increasing the bond wire inductance on the differential pair branch containing the laser-driver. To maintain good transient characteristics this inductance must be kept to a minimum.

Measurement Results

In this chapter the measurement results for the Linear-Driver IC are presented.

LASER-DIODE BIAS CURRENT

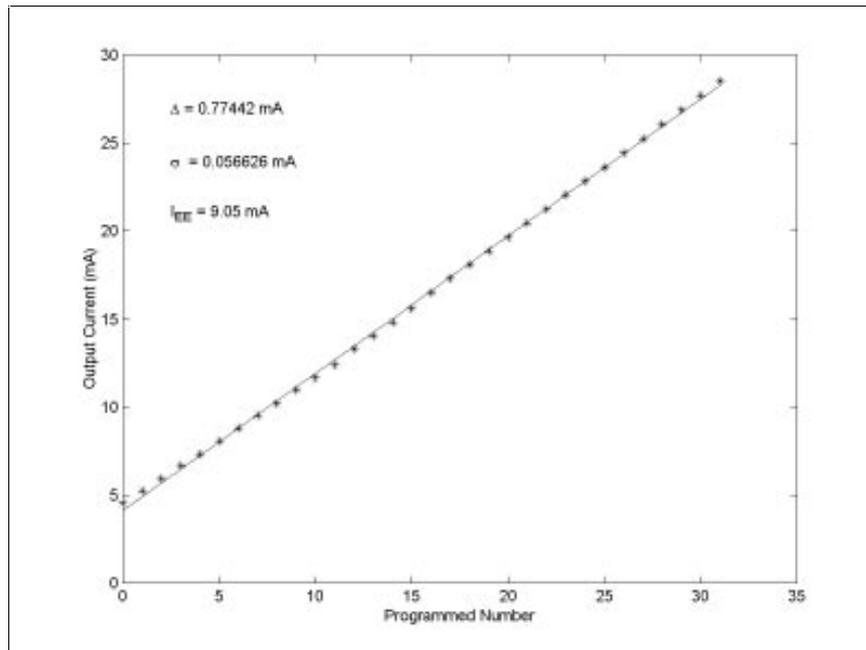


Figure 11 Measured laser-diode quiescent current as function of the number programmed in the “bias-current programming register” (see I²C Interface)

Number (H)	I _{bias} (mA)						
00	4.5	08	10.2	10	16.3	18	22.5
01	5.2	09	11.0	11	17.1	19	23.3
02	6.0	0A	11.7	12	17.9	1A	24.1
03	6.7	0B	12.4	13	18.7	1B	24.9
04	7.4	0C	13.2	14	19.4	1C	25.7
05	8.1	0D	13.9	15	20.2	1D	26.5
06	8.8	0E	14.7	16	21.0	1E	27.3
07	9.5	0F	15.4	17	21.8	1F	28.1

Table 1 Approximate values of the laser-diode quiescent current as function of the laser-diode bias current programming number

DC TRANSFER CHARACTERISTIC (E/E)

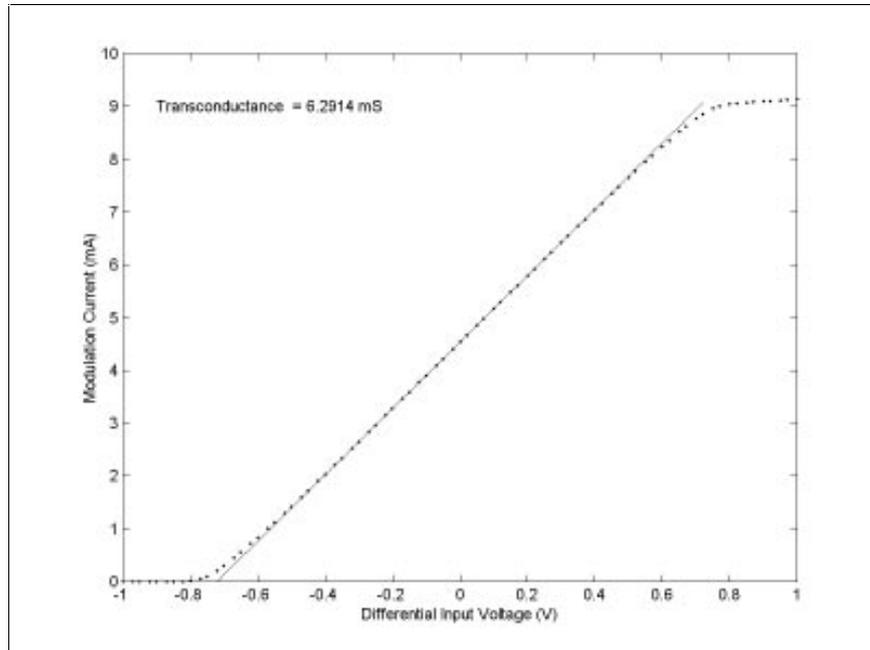


Figure 12 Measured DC transfer function – electrical/electrical measurement

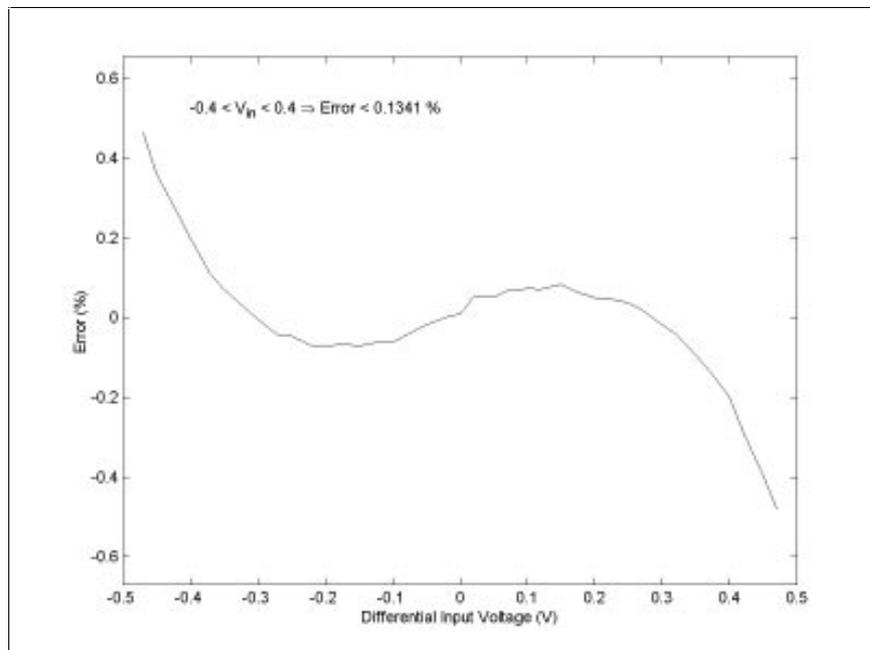


Figure 13 Measured Integral nonlinearity – electrical/electrical measurement

DC TRANSFER CHARACTERISTIC (E/O/E)

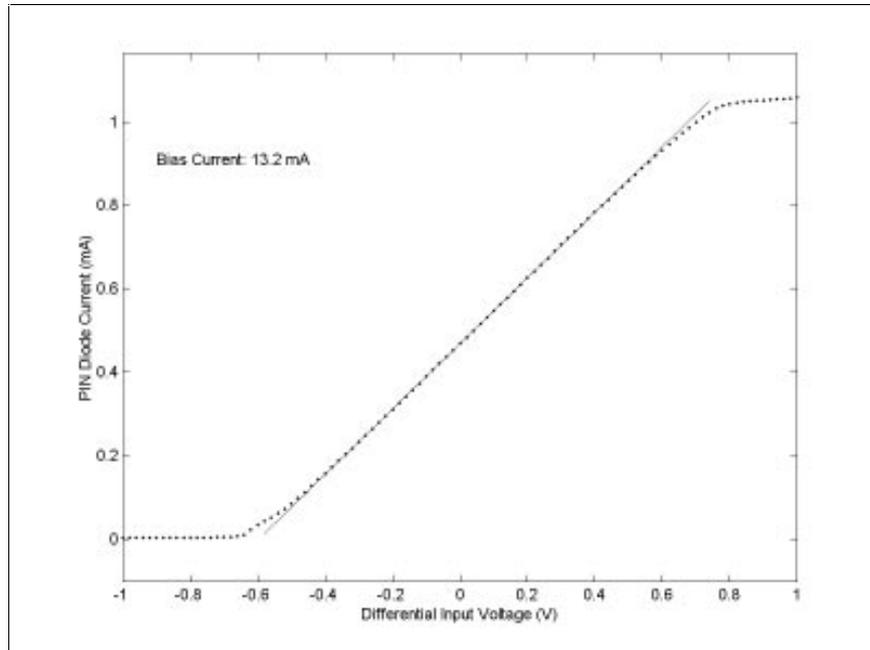


Figure 14 Measured DC transfer function – electrical/optical/electrical measurement

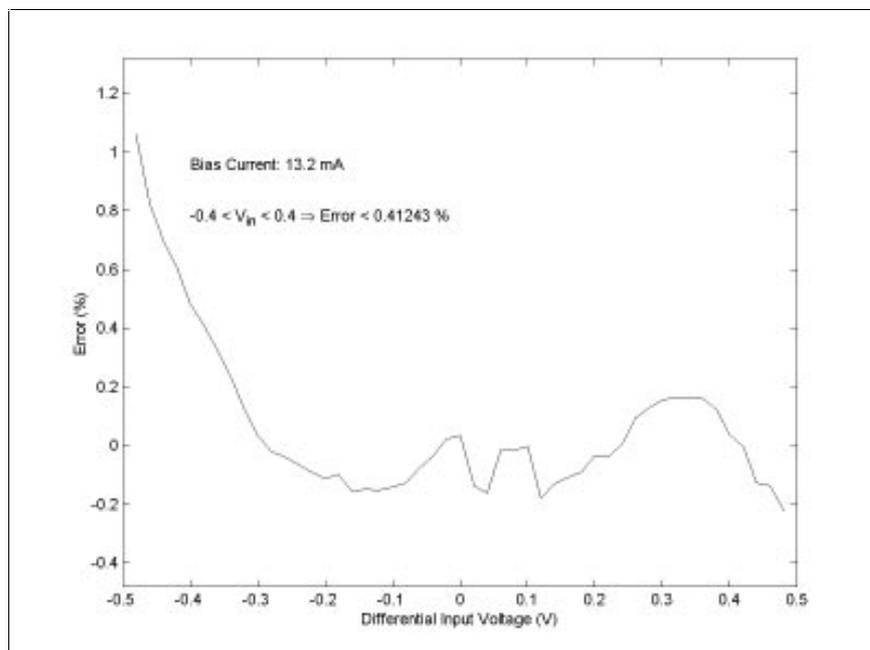


Figure 15 Measured Integral nonlinearity – electrical/optical/electrical measurement

COMMON MODE

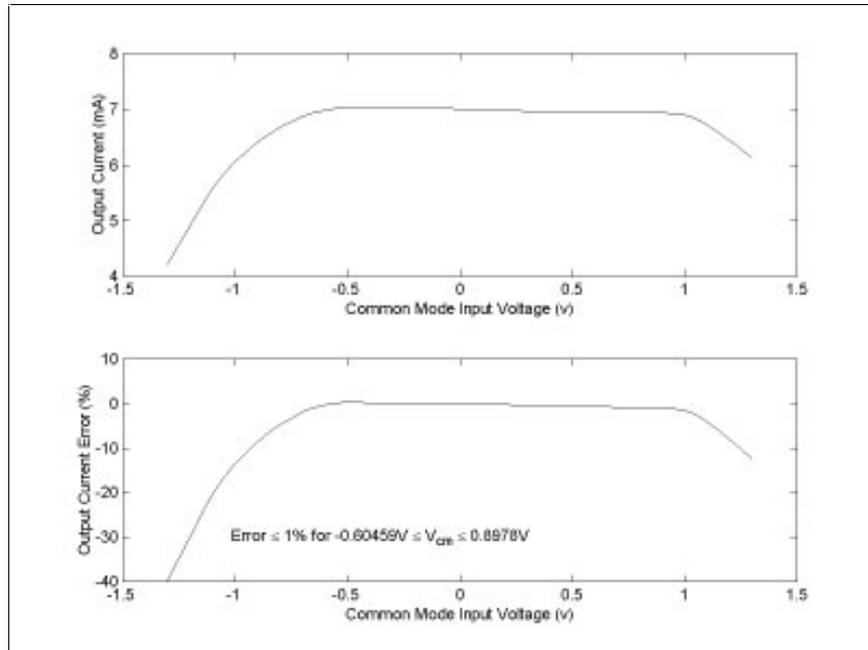


Figure 16 Output current (top) and output current error (bottom) versus the input common mode voltage. Differential input voltage +400 mV

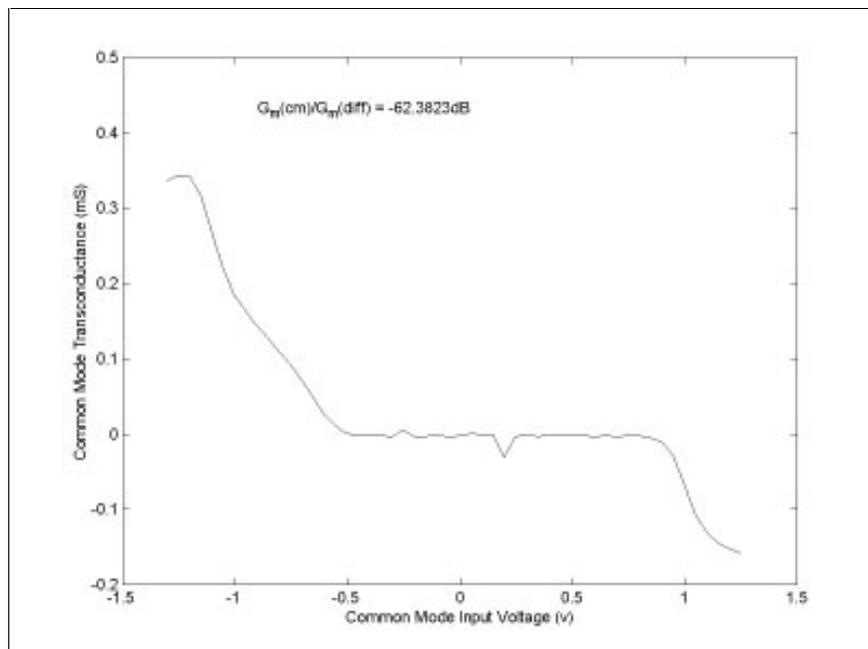


Figure 17 Common mode gain as function of the input common mode voltage. Differential input voltage +400 mV

PULSE RESPONSE (E/O/E)

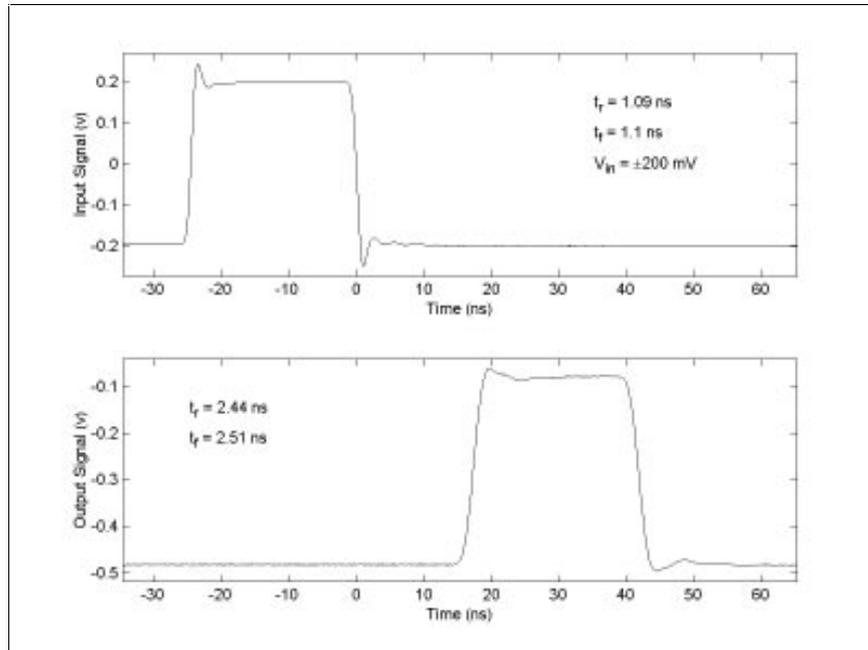


Figure 18 Pulse response (bottom) for an input signal (top) with 1 ns raise and fall times – electrical/optical/electrical measurement

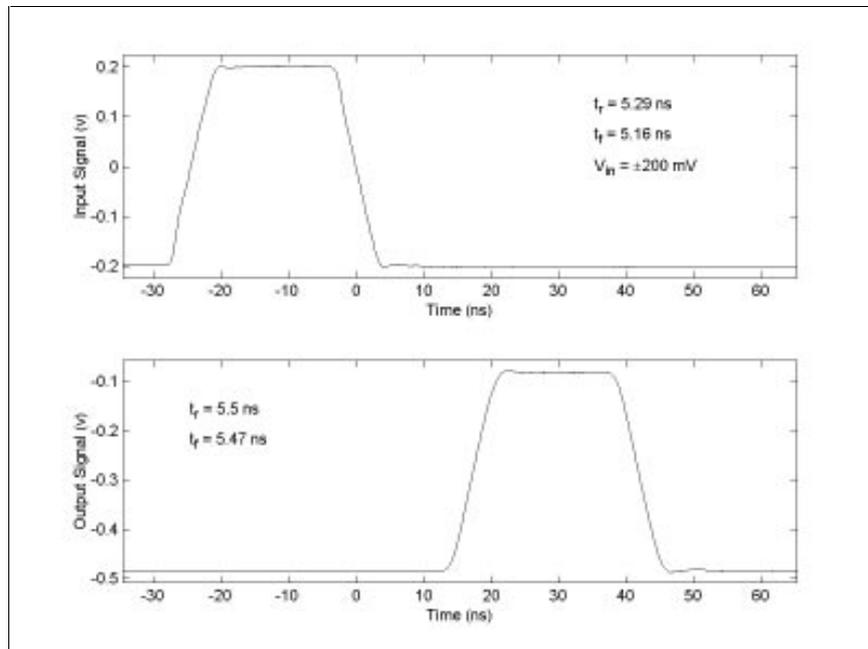


Figure 19 Pulse response (bottom) for an input signal (top) with 5 ns raise and fall times – electrical/optical/electrical measurement

CROSSTALK (E/O/E)

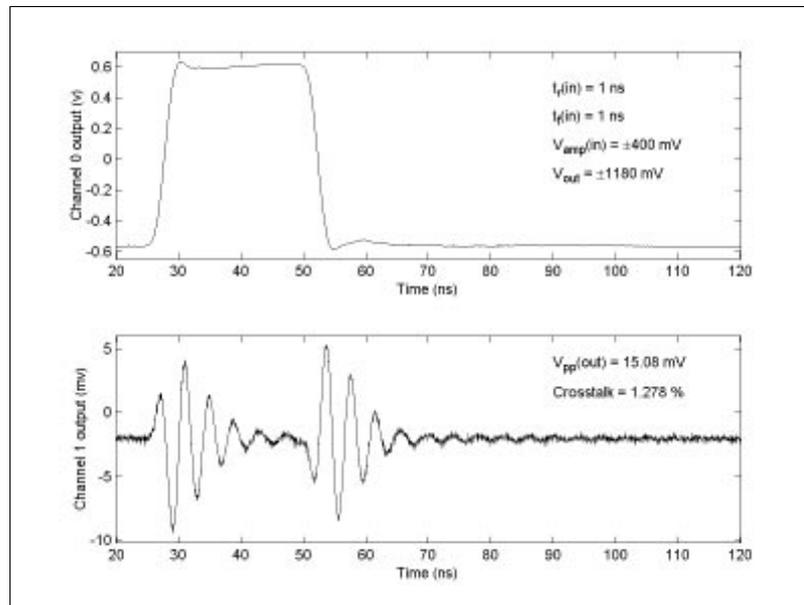


Figure 20 Measured crosstalk signal on channel 1 when an 1 ns fall and rise time input signal is applied to channel 0: Channel 0 response (top) and crosstalk signal on channel 1 (bottom) – electrical/optical/electrical measurement

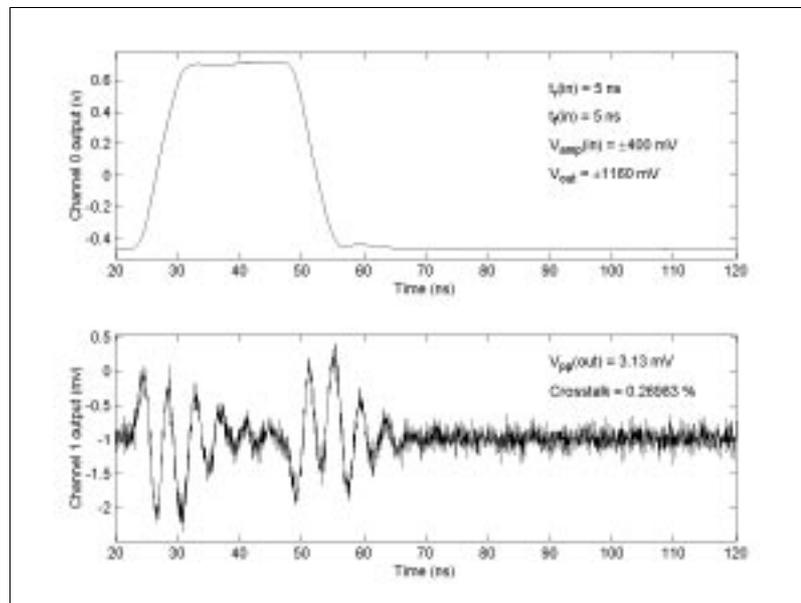


Figure 21 Measured crosstalk signal on channel 1 when an 5 ns fall and rise time input signal is applied to channel 0: Channel 0 response (top) and crosstalk signal on channel 1 (bottom) – electrical/optical/electrical measurement

NOISE

The equivalent input noise voltage was measured to be 2.0 mV and 4.5 mV for minimum and maximum laser-diode bias current, respectively. These values are higher than the goal of 1 mV (for maximum bias) and considerably higher than the simulated values of 0.3 mV (minimum bias) and 1.1 mV (maximum bias). Figure 22 summarises the Laser-Driver main noise contributions. The figure shows that 85% of the total noise contribution is due to the bias circuit. This happens because a large current gain exists between the bias circuit and the output of the driver: For the present circuit a current gain of 100 is necessary to bias the output stage and currents gain up to 260 are necessary to generate the laser-diode bias current. Note that, the noise current generated by the bias circuit undergoes through the same gain mechanisms than the power supply noise that is coupled to the output through the bias circuit (see Output Stage Power Supply).

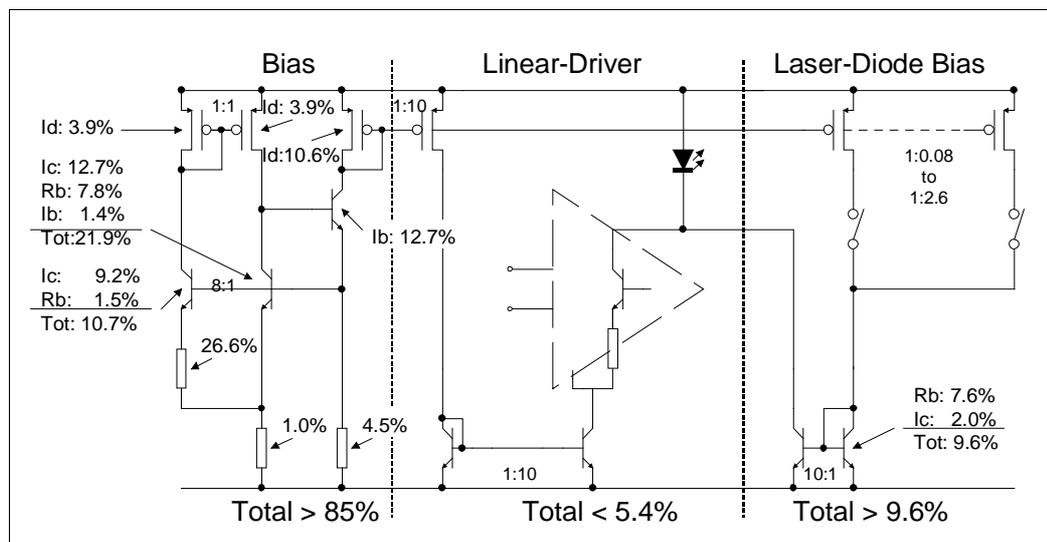


Figure 22 Summary of the main noise contributions

Appendix

Transconductance Linearisation

In this appendix, a first and second order approximations to the large signal transconductance of the emitter-coupled pair with emitter degeneration resistors are developed. Using the second order approximation criteria to choose the value of the emitter resistors that achieve a certain degree of linearisation of the transconductance are established.

EMITTER-COUPLED PAIR TRANSCONDUCTANCE

The differential pair has been extensively used as the output stage in laser driver circuits for digital communications [11]. The differential pair structure is an attractive output stage because, it allows a good control of the laser modulation current and, due to its symmetrical structure, only low noise currents are injected in the power supply, a feature that is particularly important for integrated arrays of transmitters. However, the large signal transconductance of the emitter-coupled pair is strongly non-linear preventing its use for analogue transmission applications without the help of some linearisation technique. The most commonly used technique employed for transconductance linearisation of bipolar differential pairs is the use of emitter degeneration resistors.

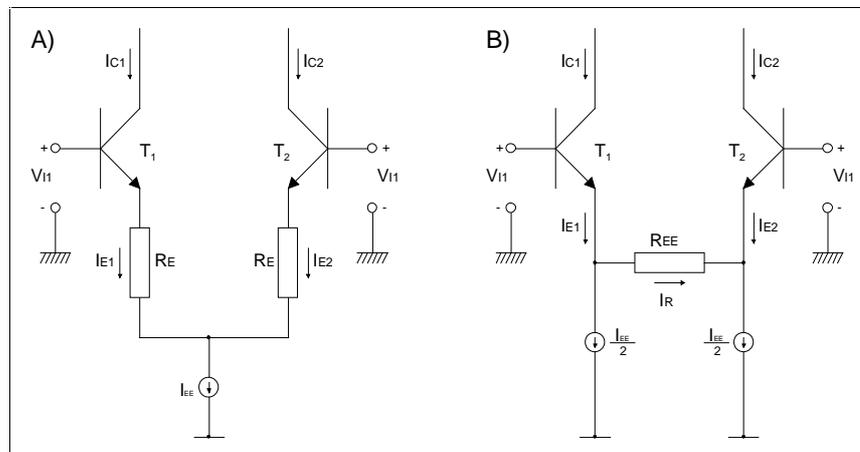


Figure 23 Emitter-coupled pairs with emitter degeneration resistors

Two emitter-coupled pair topologies – which include emitter degeneration resistors – are represented in Figure 23. The large signal transconductance of both structures in Figure 23 have the same behaviour provided that resistor R_{EE} in topology B) is made equal to $2 \times R_E$ where, R_E is the emitter degeneration resistor in topology A).

All the derivations that will be made are for circuit A). The derived results are however also valid for topology B) provided that $R_{EE} = 2 \times R_E$.

To obtain the differential pair transconductance, we start by summing the voltages around the input loop and the currents at the emitter degeneration resistors node (topology A):

$$V_d + R_E(I_{e2} - I_{e1}) + V_{be2} - V_{be1} = 0 \quad (1)$$

$$I_{EE} = I_{e1} + I_{e2} \quad (2)$$

Where $V_d = V_{i1} - V_{i2}$, V_{be1} and V_{be2} are the base emitter voltage drops in transistors T_1 and T_2 , respectively. All the other symbols are defined in Figure 23. Form the Ebers-Moll equations [12]:

$$V_{be1} = V_T \ln\left(\frac{I_{c1}}{I_S}\right) \quad (3)$$

$$V_{be2} = V_T \ln\left(\frac{I_{c2}}{I_S}\right) \quad (4)$$

provided that $V_{be1}, V_{be2} \gg V_T$. In equations (3) and (4) V_T is the thermal voltage and I_S is the saturation current [12] which it is assumed to be the same for both transistors. Equation (2) can be written in terms of the collector currents using the common-base configuration current gain⁴ α_F :

$$I_{EE} = \frac{1}{\alpha_F}(I_{c1} + I_{c2}) \quad (5)$$

Replacing equations (3) and (4) in (1), expressing I_{c2} in terms of I_{c1} and I_{EE} and simplifying we arrive at:

$$\frac{V_d}{V_T} + \frac{R_E}{\alpha_F V_T}(\alpha_F I_{EE} - 2I_{c1}) + \ln(\alpha_F I_{EE} - 2I_{c1}) - \ln(I_{c1}) = 0 \quad (6)$$

This equation can now be solved numerically to obtain the transconductance function $I_{c1} = G(V_d)$ for different values of the circuit parameters. However, the numerical solution of equation (6) does not provide insight into how the different circuit parameters affect linearity. To gain this insight we will now develop first and second order approximations to the large signal transconductance of the emitter-coupled pair with emitter degeneration resistors.

⁴ Note that the dependence of the common-base current gain with the collector current is being neglected.

First and Second Order Approximations

Due to circuit symmetry the collector currents can be expressed as:

$$I_{c1} = \frac{\alpha_F I_{EE}}{2} + i \quad (7)$$

$$I_{c2} = \frac{\alpha_F I_{EE}}{2} - i \quad (8)$$

where, $\frac{\alpha_F I_{EE}}{2}$ is the collector current when $V_d = 0$ and i is the difference between the collector current and $\frac{\alpha_F I_{EE}}{2}$. The current i is thus constrained to take values between $\pm \frac{\alpha_F I_{EE}}{2}$. Replacing equations (7) and (8) in (6) we obtain,

$$\frac{V_d}{V_T} - \frac{2R_E i}{\alpha_F V_T} + \ln\left(\frac{\alpha_F I_{EE}}{2} - i\right) - \ln\left(\frac{\alpha_F I_{EE}}{2} + i\right) = 0 \quad (9)$$

and simplifying we arrive at:

$$\frac{V_d}{V_T} - \frac{2R_E i}{\alpha_F V_T} + \ln\left(1 - \frac{2i}{\alpha_F I_{EE}}\right) - \ln\left(1 + \frac{2i}{\alpha_F I_{EE}}\right) = 0 \quad (10)$$

Since $\left|\frac{2i}{\alpha_F I_{EE}}\right| \leq 1$ the logarithmic functions in equation (10) can be expanded in power series of the form:

$$\ln(1+x) \cong x - \frac{x^2}{2} + \frac{x^3}{3} - \dots \text{ for } -1 < x \leq 1 \quad (11)$$

$$\ln(1-x) \cong x - \frac{x^2}{2} - \frac{x^3}{3} - \dots \text{ for } -1 \leq x < 1 \quad (12)$$

Keeping the first three terms in the power series expansion the difference between the logarithms can be written as:

$$\ln(1-x) - \ln(1+x) \cong -2x - \frac{2x^3}{3} \text{ for } -1 < x < 1 \quad (13)$$

Using (13) equation (10) can be approximated by:

$$\frac{V_d}{V_T} - \frac{2R_E i}{\alpha_F V_T} - \frac{4i}{\alpha_F I_{EE}} - \frac{2}{3} \left(\frac{2i}{\alpha_F I_{EE}} \right)^3 \cong 0 \text{ for } \left| \frac{2i}{\alpha_F I_{EE}} \right| < 1 \quad (14)$$

The above equation can be rewritten as

$$i = \frac{1}{\frac{2R_E}{\alpha_F V_T} + \frac{4}{\alpha_F I_{EE}} + \frac{16i^2}{3(\alpha_F I_{EE})^3}} \times \frac{V_d}{V_T} \quad (15)$$

A first order approximation to the transconductance function can be obtained from equation (15) by discarding the third term in the denominator resulting in:

$$i = \frac{1}{\frac{2R_E}{\alpha_F V_T} + \frac{4}{\alpha_F I_{EE}}} \times \frac{V_d}{V_T} \quad (16)$$

It is useful to normalise equations (15) and (16) to the maximum collector current. In this case we obtain for the second order approximation,

$$i_n = \frac{i}{\alpha_F I_{EE}} = \frac{1}{\frac{2R_E I_{EE}}{V_T} + 4 + \frac{16}{3} i_n^2} \times \frac{V_d}{V_T} \quad (17)$$

and for the first order:

$$i_n = \frac{i}{\alpha_F I_{EE}} = \frac{1}{\frac{2R_E I_{EE}}{V_T} + 4} \times \frac{V_d}{V_T} \quad (18)$$

Transconductance Error

Equation (15) can be interpreted as a “linear” dependence between the differential input voltage and the collector current. However, its constant of proportionality – the transconductance – depends on the current level it self introducing an error in the ideal linear behaviour given by equation (16). In order to be able to quantify this error we define the relative transconductance error as:

$$S_{err}(i_n) = \left| \frac{G_{app}(i_n) - G_{lin}}{G_{lin}} \right| = 1 - \frac{G_{app}(i_n)}{G_{lin}} \quad (19)$$

where $G_{app}(i_n)$ and G_{lin} are the transconductance functions obtained from equations (17) and (18) respectively. As an example, Figure 24 shows the collector current obtained from equation (6), (17) and (18) when the voltage drop across the emitter resistor is equal to five times the thermal voltage. The rectangle in the figure indicates the range of input voltages and output currents where the relative transconductance error is less than 5%.

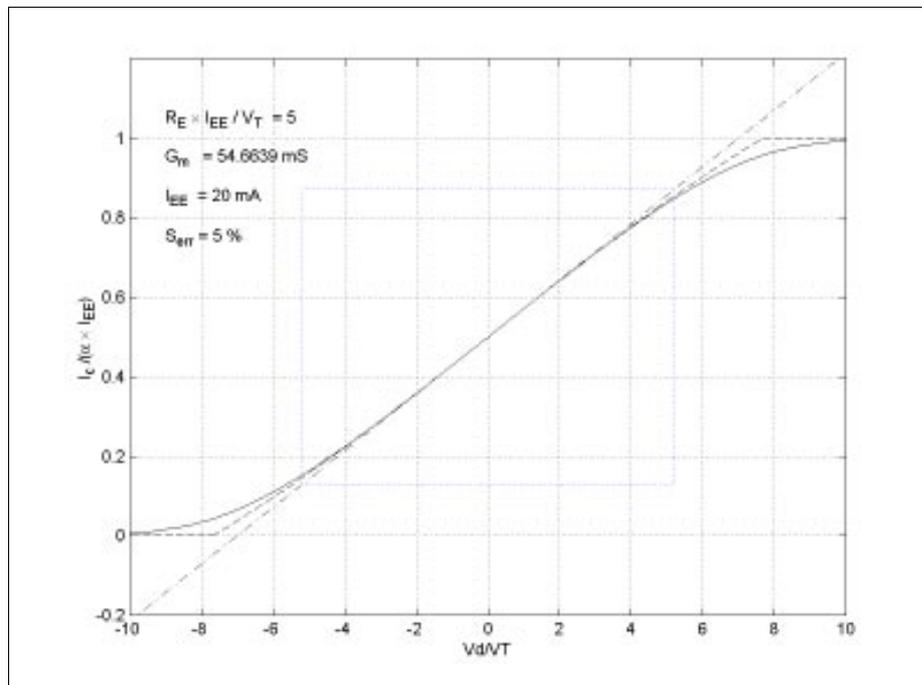


Figure 24 Normalised collector current: equation (6) (solid line), second order approximation (dashed line) and linear approximation (dash-dot line). The drawn rectangle indicates the range of input voltages and output currents where the relative transconductance error is less than 5%.

Output Current and Input Voltage Ranges

As can be seen from Figure 24 there is a limited range of output currents and input voltages that satisfy a given transconductance linearity. From equations (17), (18) and (19) the maximum collector current compatible with the relative transconductance error S_{err} is:

$$|i_n| \leq i_{n,max} = \frac{1}{2} \sqrt{\frac{3S_{err}}{1-S_{err}} \left[\frac{R_E I_{EE}}{2V_T} + 1 \right]} \quad (20)$$

This means that only a fraction of the total available collector current (equal to $2 \times i_{n,max}$) can be usefully used to linearly modulate the laser⁵.

The allowed range of input voltages is now easily obtained from equations (20) and (18) and is given by:

$$\left| \frac{V_{d,max}}{V_T} \right| = \left[2 \times \frac{R_E I_{EE}}{V_T} + 4 \right] i_{n,max} \quad (21)$$

Figure 25 and Figure 26 are plots of equations (20) and (21), respectively, as function of the product $R_E I_{EE}$. In both figures the relative transconductance error is used as a parameter.

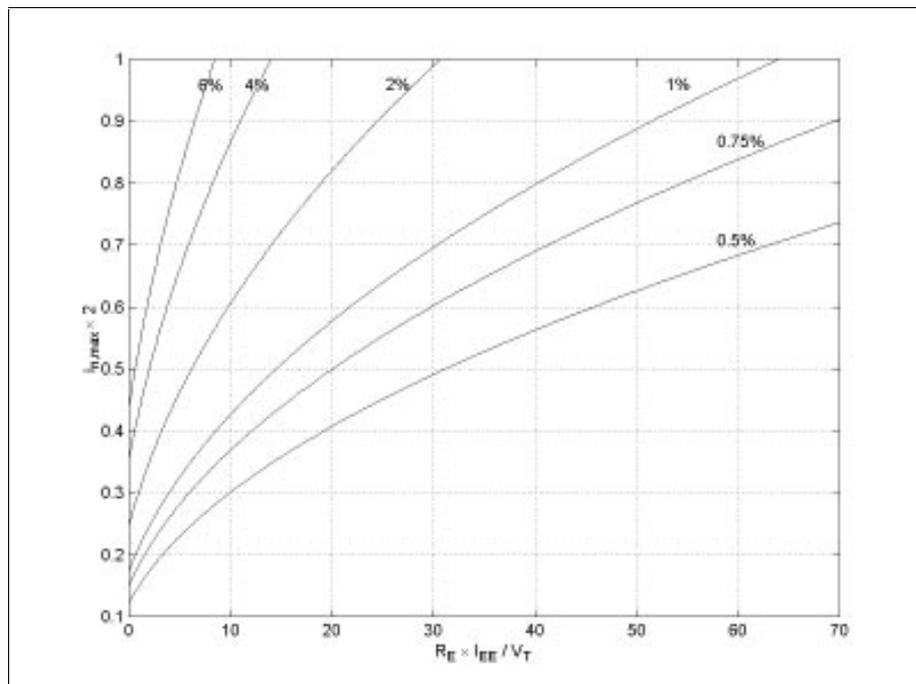


Figure 25 Normalised collector current range as a function of the normalised voltage drop across the emitter degeneration resistor and the relative transconductance error.

⁵ We will call this range the collector current modulation efficiency.

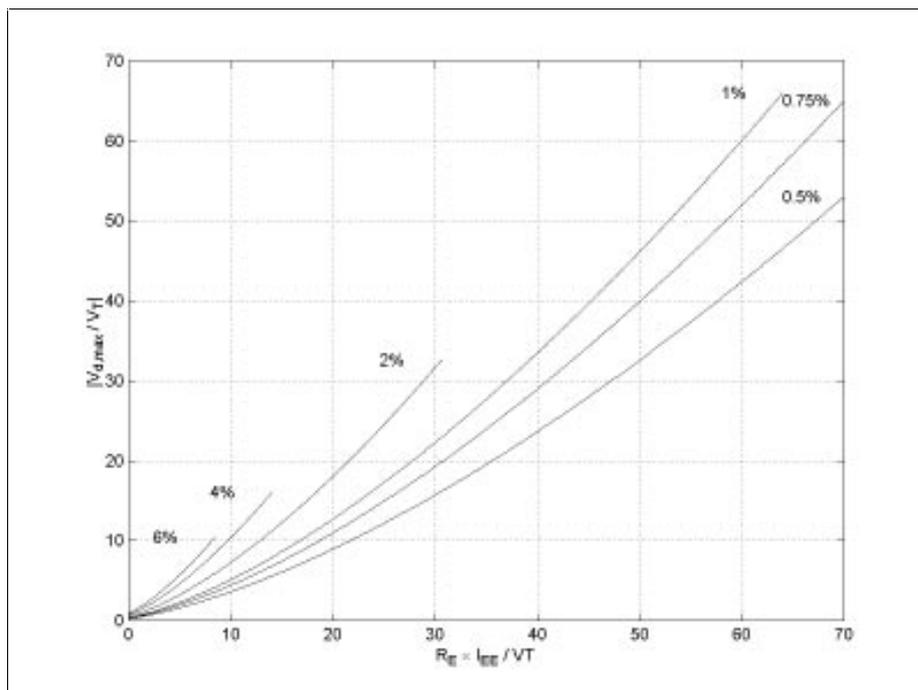


Figure 26 Normalised input voltage range as a function of the normalised voltage drop across the emitter degeneration resistor and the relative transconductance error.

Equations (20) and (21) show clearly that of the four parameters, S_{err} , $V_{d,max}$, $i_{n,max}$ and $R_E \times I_{EE}$ (Figure 25 and Figure 26) only two can be chosen independently.

For instance, once the transconductance linearity and the input voltage range are specified, the voltage drop across the emitter resistors and the collector current modulation efficiency are automatically determined. This means that in a single amplifying stage it might not be possible to satisfy all the design specifications. In general, a voltage gain stage followed by a transconductance stage will be required to satisfy all the design parameters. In the case of a laser-driver the output stage will be typically the most power hungry stage in the circuit. It should thus be designed to maximise the collector current modulation efficiency. A previous stage will provide voltage gain to adapt the linear range of this stage to the input signal range.

It is clear that increasing the collector current modulation efficiency and the linear modulation input range can only be achieved by increasing the voltage drop across R_E . However, this reduces the input voltage common mode range by $R_E I_{EE}$. Also, as can be seen from equation (18), the increased linearity for a given tail current can only be obtained at the cost of decreased transconductance. Additionally, the designer has to take into account the noise performance degradation of the differential pair with the increase of R_E in low noise designs.

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