Simulation and characterisation of the CMS tracker optical readout chain

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Abstract - *The CMS tracker readout will make use of analogue optical links. In order to simulate and characterise their functionality within a complete readout chain, a software program has been developed in a LabVIEW environment. It allows for interchangeability of software modules and real hardware components so that both full software simulation and mixed hardware/software characterisation of the chain are possible. We present results obtained with a single channel readout chain prototype, where the front-end signals are emulated and the rest of the chain (from laser driver to digitising elements) are real hardware components.*

1. Introduction

The CMS tracker readout chain will make use of optical links to transmit pre-processed analogue information from the front-end chips (APVs) to the front-end drivers (FEDs) [1]. This chain can be partitioned into blocks (APV, optical link, FED), which are individually developed and evaluated by different groups working in parallel. The APV chip [2], among other functions, serialises the data corresponding to 128 detector channels on a single analogue output at a 20MS/s rate. Data from two parallel APV chips are interleaved by a multiplexer (MUX) on one optical channel, so that the resulting transmission rate is 40MS/s. The optical links [3] transfer analogue data to a distant site, by directly modulating 1300nm edge-emitting laser diodes. At the back-end of the link, InGaAs photodiodes detect the modulated light and convert the information back to electrical. The FED [5] digitises the hits with an ADC and stores the results in a local memory until they are required by the data acquisition and higher level triggering system.

To evaluate individual hardware blocks in a realistic environment the emulation of the rest of the chain is required. Moreover, the analysis of system issues such as noise, parameter spread, crosstalk, and calibration strategies, requires the simulation of the whole chain. We have chosen a software oriented approach to match these needs. Each element of the chain (optical link included) is either simulated or interfaced to software modules via A/D and D/A

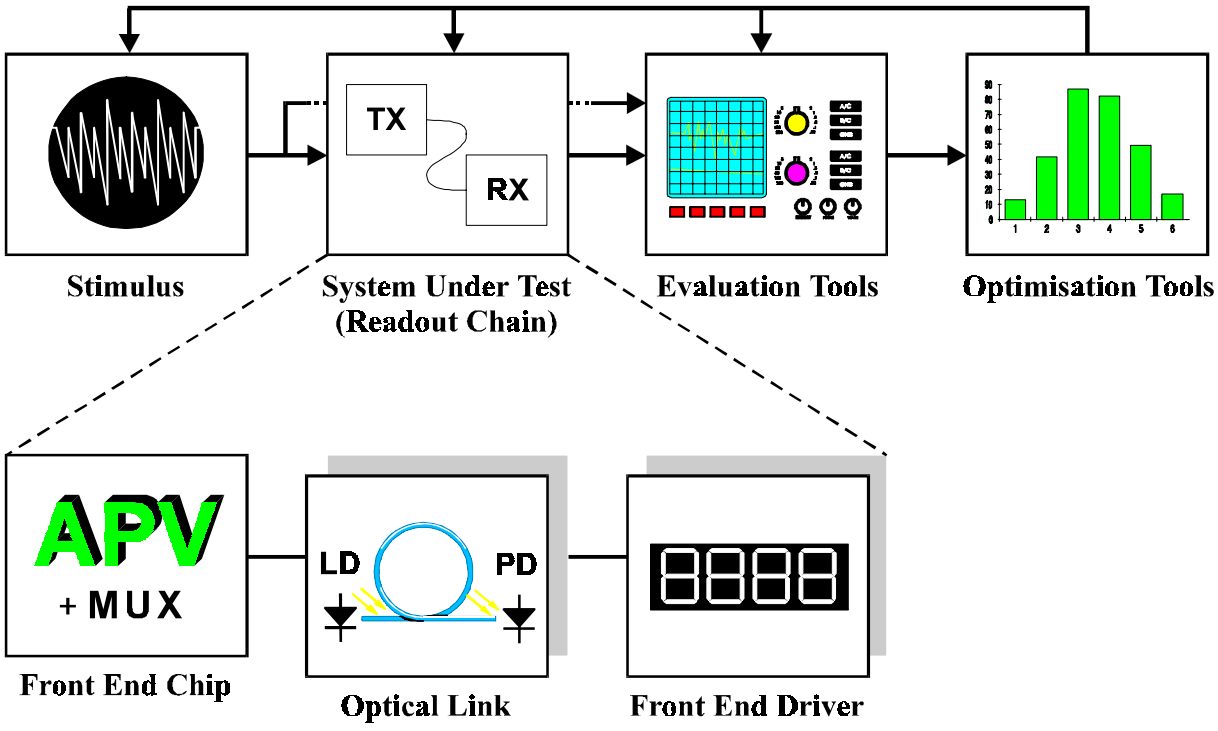


Figure 1: *Block diagram of the system simulation, evaluation, and optimisation tools. In the present "system under test" configuration, the optical link and FED hardware prototypes are operational (shadowed blocks), whereas the APV chip is only simulated (non-shadowed block).*

converters. Thanks to a uniform interface to the simulated blocks and to the interfaces to real blocks, both mixed software/hardware and full software simulations can be performed in a LabVIEW-based environment. Evaluation criteria and results presentation are also uniform, so that direct comparison of simulated and experimental results is straight forward.

Typical applications range from simple characterisation of a hardware module (or group of modules), to system level simulation, algorithm prototyping, and investigation of alternative concepts. Hereby, we present the characterisation of the readout chain prototype (from the optical link to the FED) with calibration or APV signals emulated with an Arbitrary Waveform Generator (AWG) as D/A converter.

2. Software environment

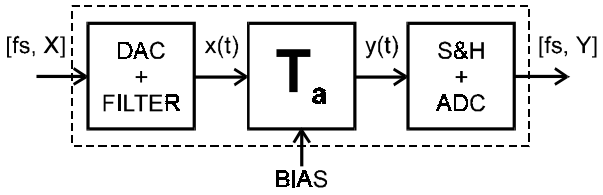
The general synoptic diagram of the program is represented in Fig. 1. Four major blocks can be identified: the stimulus block, the system-under-test block, the evaluation block, and the optimisation block. Each of them consists of a collection of modules, which can be interchanged and combined according to the particular application to be developed. The stimulus block provides reference signals to pass to the input of the system-under-test block. The system-under-test block generates the system response corresponding to a given stimulus, according to system characteristics. The evaluation block compares system responses to the corresponding stimuli and calculates evaluation parameters. The optimisation block gathers evaluation parameters corresponding to repeated calls to the evaluation block (for different channels, different parameter settings, or different times) and generates statistics, optimisation, or time evolution graphs.

2.1 System model

The system under test is in general described as a cascade of simpler unidirectional transmission blocks, as shown in Fig. 1 (APV, optical link, FED). The basic building block, is either an interface to the real system prototype (hardware block) or a purely mathematical representation of it (software block).

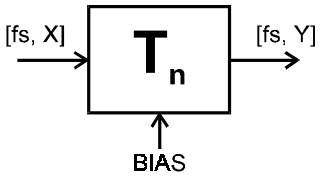
In an hardware block, D/A and A/D converters are used, at the input and output of the block respectively (see Fig. 2a), to convert back and forth between digital and analogue, time-sampled and time-continuous domains. In practice, either the internal converters of digital testing equipment or independent VME modules are used as interfaces, and are read or written via a communication bus.

In a software block, static, dynamic and noise performance are simulated numerically (see Fig. 2b).



$$y(t) = T_a \{ x(t); BIAS \}$$

(a)



$$[fs, Y] = T_n \{ [fs, X]; BIAS \}$$

(b)

Figure 2: *Principle of the mixed hardware/software simulation: the system building blocks are either purely software blocks simulating the system performance (b), or numerical interfaces to the real system block (a).*

Static performance (gain, nonlinearity) is simulated by a simple memoryless equation relating the input to the output. Dynamic performance (frequency selectivity, time delay) is simulated by numerical filters of different order and type. Complex filters are built by cascading simpler low-order filters. Noise performance is simulated by additive sources inserted along the chain.

The model provides access to all parameters affecting system specifications and operational modes ('bias', in Fig. 2), such as gains and bandwidths as well as working points and offsets. It is therefore well suited to perform Montecarlo simulation and system oriented analysis and optimisation.

In our present set-up, the hardware of the optical link and of the FED are operational in the laboratory, whereas the APV+MUX chip is only simulated.

2.2 Evaluation tools

The evaluation block quantifies the system performance in terms of static and dynamic behaviour, as well as noise budget.

A full static characteristic is acquired by scanning the system input and monitoring its output. The system gain is defined as the slope of a regression line. The definition of the regression method best applied to realistic system calibration procedures is under study. The nonlinearity error is the absolute difference between the real output and its regression. It is

therefore a function of the input level. The rms noise is also evaluated as a function of the input level.

The dynamic performance of the system is evaluated by sending broad band signals at the input. Deconvolution of the system response allows to extract the ideal pulse and step responses, as well as the transfer function. All the dynamic parameters of interest can then be evaluated: response time (rise, fall, settling), stability (overshoot, ringing), cut-off frequency, time delay.

2.3 Optimisation tools

The use of the optimisation block implies iterated calls to the other blocks. The parameters controlling the other blocks (stimulus parameters, system bias, type of evaluation) can be adjusted between measurements. The possible applications can be classified in four groups: statistical analysis (Montecarlo simulation), long term monitoring, parametric analysis, and algorithm prototyping.

1. Montecarlo simulations are performed by randomly generating the parameters for either the stimulus block or the system block, according to the application. The stimulus block can for instance output quasi-random signals and simulate a realistic detector in a beam-test environment, while the system block can simulate the statistical interplay between device tolerances and their effect on global system parameters.
2. The system can be monitored over long periods of time. Environmental parameters (temperature, B-field, radiation dose) can be swept and correlation with system performance can be studied [6]. Alternatively, in a stable environment, the intrinsic time stability of the system can be evaluated [7].
3. By sweeping a restricted set of parameters (ex: laser bias, damping capacitance), the system performance can be analysed as a function of those parameters, and an optimum working point can be defined.
4. The program versatility can be exploited for the investigation of new concepts and for the prototyping of new blocks, before time is invested in their design and realisation. Possible developments include: laser threshold tracking, gain calibration, channel equalisation, signal compression, etc.

3. Readout chain characterisation

The tools described in the previous section have been applied to the characterization of a readout chain including a real optical link [4] and FED. The simulation tools have been used both for mixed hardware/software simulation (interface to the real system) and purely software simulation (APV+MUX output sequence). The evaluation tools have been used for static and dynamic evaluation of the system. The optimization tools have been used for skewing the clock and optimize sampling sampling.

3.1 Experimental setup

The laboratory setup for the full readout chain characterisation is depicted in figure Fig. 3. Data and timing signals are generated by an AWG, providing 1 analogue and 2 digital outputs.

The optical link is configured as described in [4], but using a laser diode with a lower efficiency (0.06W/A). The laser threshold current is 10mA. The link settings are such that an input range between -400mV and +400mV at the level of the laser driver corresponds to an output range between 0 and 3V at the level of the photoreceiver (matched to the ADC input). In this conditions, the laser diode is biased between 13mA and 17mA, and generates a CW optical power between 180µW and 420µW. The optical link output is terminated with a 50Ω resistance in parallel to the ADC output. An additional 50Ω series resistance is mounted between the receiver and the termination to minimize reflections, in case a coaxial cable has to be driven to monitor the link output with a scope. This arrangement results in a 50% drop in output signal

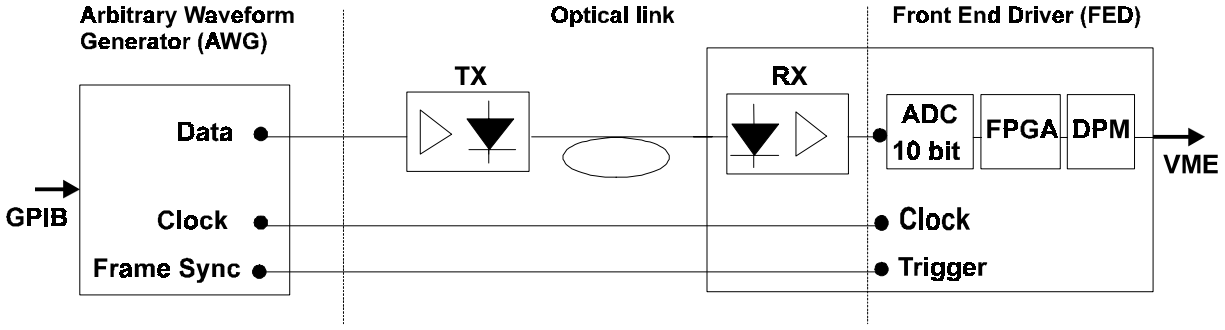


Figure 3: *Characterisation of the optical readout chain, from arbitrary waveform generator and optical link to front end driver.*

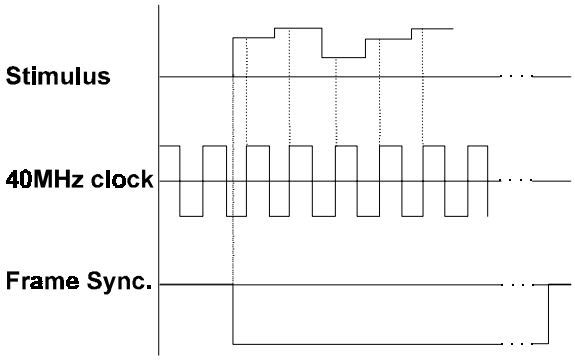


Figure 4: *Data and timing signals generated by the AWG.*

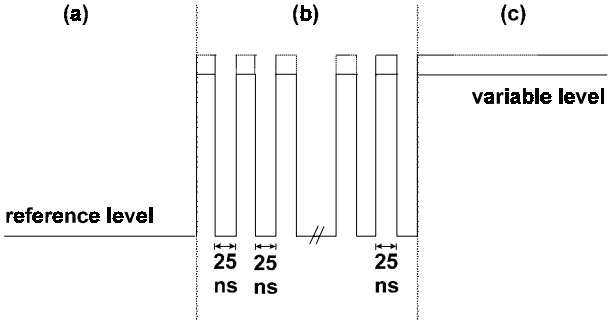


Figure 5: *Stimulus for the readout chain characterisation (160 samples long, to match FED readout format).*

level, but will not be present in the final system configuration.

The CMS prototype Frond End Driver board [5] is housed in a 9U VME crate. It contains the photodiode receiver part of the optical link, along with a 10-bit, 40MS/s ADC mounted on a FPGA daughter card. It digitises the analogue data transmitted by the link and stores data samples in a Dual Port Memory (DPM) before VME readout (Fig. 3 on the right).

The software configuration [8] of the FED and FPGA determines the data format expected by the FED, as well as the digitisation rate of the ADC. In our setup, the FPGA is operated in scope mode (no post-processing) at 40MS/s and is configured to readout 160 samples per event. This is based on a single APV-chip readout format [7], with 32 digital samples followed by 128 analogue samples. A typical APV event is shown in Fig. 8. A simulated 1MIP signal is visible on channel 40, superposed to the corresponding pedestal.

The output of the AWG is controlled by a software generated trigger. Timing signals (clock and trigger) needed to operate the FED are provided in synchronism with the data. FED data sampling occurs at the rising edge of the clock and is strobed by the Frame Sync signal (Fig. 4).

A PowerMac 7600/120 running LabVIEW software controls both the AWG, via a GPIB bus, and the VME crate, housing the FED, via a PCI-MXI-VME interface.

Data sampling occurs at 40MS/s (FED), but stimulus signal generation (AWG) occurs at a higher frequency to allow for shaping of the waveform reconstructed by the APV+MUX emulator. Twenty points are used at a frequency of 800 MHz per point, to reconstruct a 25ns pulse duration, matching the 40MS/s digitisation rate of the FED ADC. Both APV and calibration signals are 160 samples long and match the FED expected data format.

Since the ADC sampling point is determined by the rising edge of the clock and sampling should occur after settling of the system, flexibility to shift clock and data with respect to each other is required to optimise digitisation accuracy (optimisation tools).

3.2 Static and dynamic evaluation

The static and dynamic evaluation tools, described

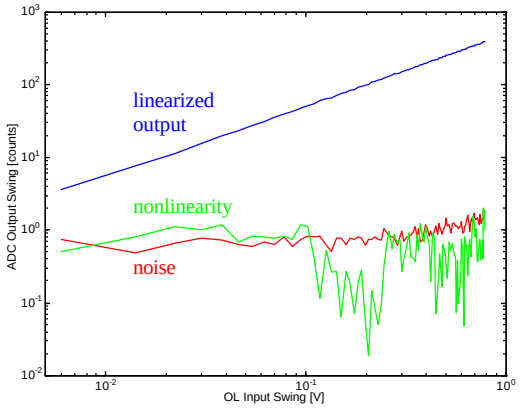


Figure 6: *Static evaluation of the readout chain. The input (output) swing is the difference between the variable level and the reference level.*

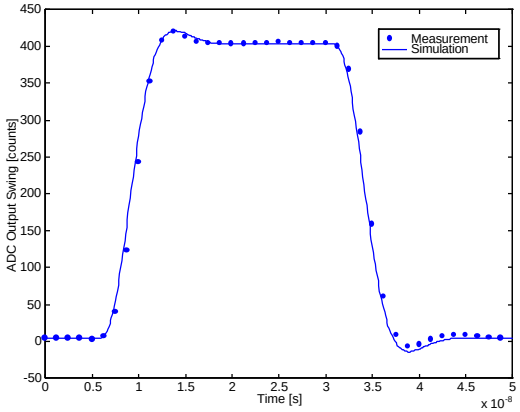


Figure 7: *Dynamic evaluation of the readout chain. The time response to an ideal input pulse is reconstructed by interleaved sampling*

in section 2, are used for the readout chain characterization. In both cases, the stimulus is the 160 samples long sequence shown in Fig. 5. The reference and variable levels (region (a) and (c) in Fig. 5), whose duration is >> 25ns, are used for evaluation of the static transfer function and of the noise. The reference level is kept constant at -400mV, while the variable level is swept between -400mV and +400mV. The constant reference level at the input of the system allows for common mode subtraction at its output. The output 'swing' (variable level - reference level) is plotted as a function of the input swing, in Fig. 6. The system gain is ~520 counts/V. The logaritmic scale is convenient to compare the signal swing level to its error components (noise and nonlinearity), and to give an immediate visual indication of the dynamic range of the system. From the graph in Fig. 6 it is apparent that the magnitude of the error components is limited to ~1 count (rms for the noise), all over the input range. The measured peak SNR is ~300:1, in agreement with the performance of the stand alone optical link prototype described in [4].

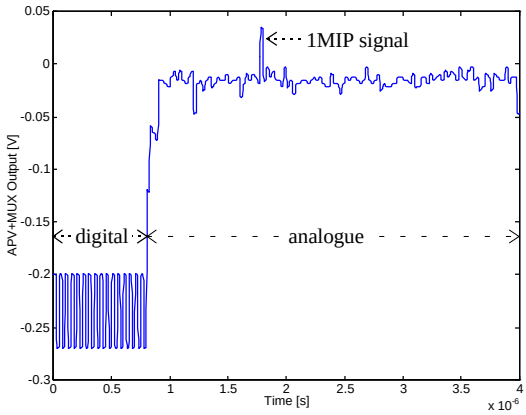


Figure 8: *APV emulation.*

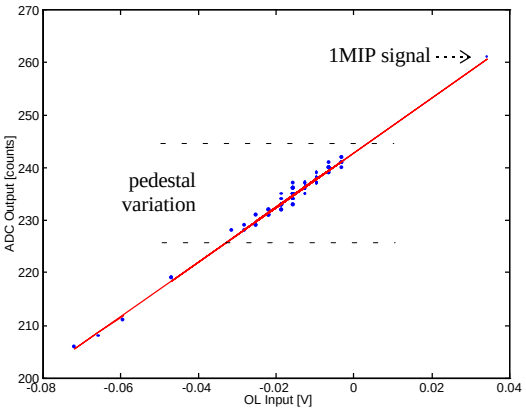


Figure 9: *Correlation between the original APV6 digital output and the FED sampled signals.*

The 25ns long alternating pulses (region (b) in Fig. 5) are used to investigate the dynamic system performance. Since the sampling rate of the FED is limited to 40MHz, interleaved sampling is needed to analyse time responses with nanosecond resolution. The same stimulus is repeatedly sent, through the chain, while the clock is being progressively skewed in steps of 1.25ns (AWG time resolution, at 800 MHz internal clock frequency). In this way, the shape of the waveform can be reconstructed with an improved time resolution. Figure 7 shows a typical reconstructed pulse response.

In a time sampled system, the most crucial parameter is the settling time, since this fixes the trade-off between speed and stability (some ringing or an over-damped response can be allowed as long as the settling time is smaller than the sampling time). The rise time is about 16-17ns, with an overshoot of 5%, corresponding to a bandwidth of 90MHz (4th order system approximation), which would be perfectly acceptable for our application.

3.3 APV6 event readout

Emulation of the APV+MUX chip requires pulse shaping of the signal before injection in the optical link. As a starting point, a file containing digitized MIP events generated by a real APV6 chip is used. The signal is then filtered through two optimally damped 100MHz second order filters, to simulate APV and MUX dynamic performance (5ns risetime, typ.). An example of pulse shaping is shown in Fig. 8, for a qualitatively optimized shift value of data versus clock signal. The emulated APV6 event is transmitted through the optical link and digitized by the FED. The correlation with the initial pulse amplitude (before shaping) is shown in Fig. 9, for the analogue information part of the signal. The 128 points are aligned on a grid, because of the finite resolution of the input and output converters. The fit slope is coherent with the measured system gain (section 3.2) of ~520 counts/V.

4. Conclusions

A software tool has been developed for system oriented mixed hardware/software simulation, evaluation, and optimisation. The tool is primarily targeted to aid in the development of the CMS tracker readout chain and to the definition of the optical link specifications. It is a versatile and expandable tool which can be used for many applications ranging from simple prototype characterisation to system level simulation, statistical and parametric analysis, as well as algorithm prototyping.

The optical link and FED hardware has been installed in our laboratory. The APV front-end chip is simulated in software, and its typical output is regenerated by an AWG. The performance of the emulated readout chain has been evaluated and the results are coherent with the measurements of a stand-alone optical link and with the accuracy of the FED ADC.

A detailed analysis still needs to be carried out, to establish practical calibration and sampling criteria. Further developments include implementation of a stand-alone master clock and trigger generator for simulation of fast (and random) triggers.

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