A Linear Laser-Driver Array for Optical Transmission in the LHC Experiments

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Abstract

A 4-way linear Laser Driver has been designed and implemented in a commercial 0.25μm CMOS technology. The full-custom IC is intended for analogue and digital data transmission as part of the 50 000 optical fibre links of the CMS particle Tracking System. Intrinsic radiation tolerance and specific design methodologies enable the device to operate over 10 years in the harsh radiation environment of the innermost LHC detectors. Although optimised for analogue operation the driver is compatible with LVDS digital signalling. A combination of linearization methods achieves good analogue performance (8-bit equivalent dynamic range with a bandwidth of 100MHz), while maintaining wide input common-mode range (±350mV) and limited power dissipation. The linearly amplified signal is added to a DC current, which can be set over a wide range (-60mA to +60mA). The latter capability allows tracking of changes in laser threshold due to ageing or radiation damage. The driver gain and bias current are set via a serial interface. Measurements have been performed on individual chips - both in isolation and in combination with prototype optical links - that confirm the full functionality of the device.

I. INTRODUCTION

The Compact Muon Solenoid (CMS) experiment [1] is one of the four colliding-beam experiments, being designed and built for operation at the CERN Large Hadron Collider (LHC). The CMS particle tracking system (or Tracker) [2] consists of 12 million channels, generating analogue samples at a 40 MHz rate. The readout electronics is shown schematically in Figure 1. The data are stored in analogue pipelines in the detector front end chips (APVs in the Figure) and – upon receipt of a first level trigger – are time-division multiplexed before transmission to the Front End Drivers (FEDs) located outside the detector. Digitisation and post-processing take place at the FED level. The data readout connection between the detector Front Ends and the FEDs is provided by 50 000 analogue optical fibre links. All the links operate synchronously with the LHC master clock (40 MHz). Because of the large number of analogue links, the electronics and opto-electronics components are primarily developed and qualified for the analogue application [3]. The same components will also be used for the digital transmission of trigger, timing, and control signals, for which 2 - 300 digital optical links are required.

All the components located within the detector volume must withstand the harsh radiation environment of the Tracker, over the nominal detector lifetime of 10 years (corresponding to a total ionising dose and hadron fluence exceeding 10 MRads and 10^{14} neutron/cm^2 respectively). Special developments and/or qualification procedures are thus needed for all electronics, devices, and materials to be used [3].

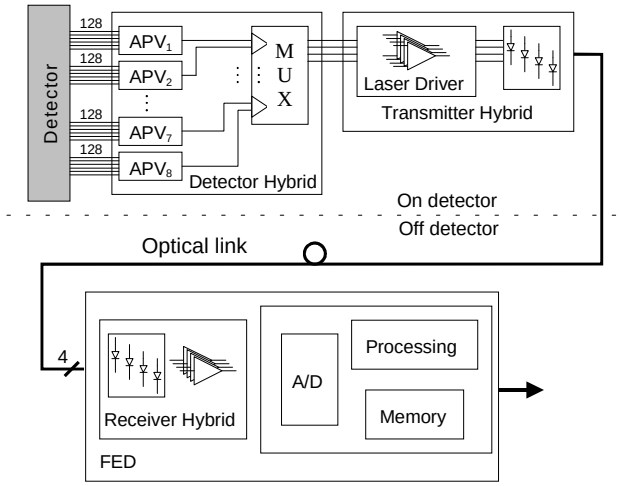

Figure 1: Tracker data-path readout architecture.

The technology for ASIC developments in the CMS Tracker is a 0.25 μm CMOS commercial technology (5 nm oxide thickness) [4]. Specific design methodologies are used to increase the circuit radiation tolerance to levels compatible with the Tracker specification. The use of this particular technology for analogue applications has been carefully evaluated for use in this application [5].

A Linear Laser Driver (LLD) array for the CMS optical links had already been developed and implemented in a non-radiation tolerant BiCMOS technology [6]. The design has now been successfully translated in the 0.25 μm CMOS technology. Section II explains the device functionality and major specifications. Section III describes the electrical circuit and layout. Sections IV to VI report on the measurement results: purely electrical measurements (Section IV), electro-optic measurements (Section V) and radiation testing for total ionising dose (Section VI).

II. FUNCTIONALITY

Figure 2 shows the block diagram of the Laser Driver chip. The laser driver converts a differential input voltage into a single ended output current added to a pre-set DC current (as shown in Figure 2-a). The DC current allows correct pre-biasing of the laser diode above threshold in the linear region of its characteristic. The absolute value of the pre-bias current can be varied over a wide range (up to 60 mA), in order to maintain the correct functionality of even severely degraded devices (i.e. laser diodes with very high threshold currents as a consequence of radiation damage). The laser diode pre-bias can be set to be positive (*source mode*) or negative (*sink mode*), thus allowing the use of both common-anode or common-cathode laser diode arrays.

Input signals are transmitted to the laser driver using ~30 cm of 100 Ω twisted pair lines. The driver is optimised for analogue operation in terms of exhibiting good linearity and low noise. However, input voltage levels are compatible with the digital LVDS standard (±400 mV into 100 Ω). The gain can be chosen from 4 pre-set values. Gain control provides an extra degree of freedom for optimally equalising the CMS Tracker readout chain. A system-level simulation of the fibre link performance achievable with a four gain equalisation is presented in [7].

The IC modularity is 4 channels per chip (Figure 2-b). About 15 000 4-way laser drivers will be used for the CMS Tracker readout and control links. The device total current must remain constant regardless of the modulation signal to minimise cross-talk and noise injection in the power supplies.

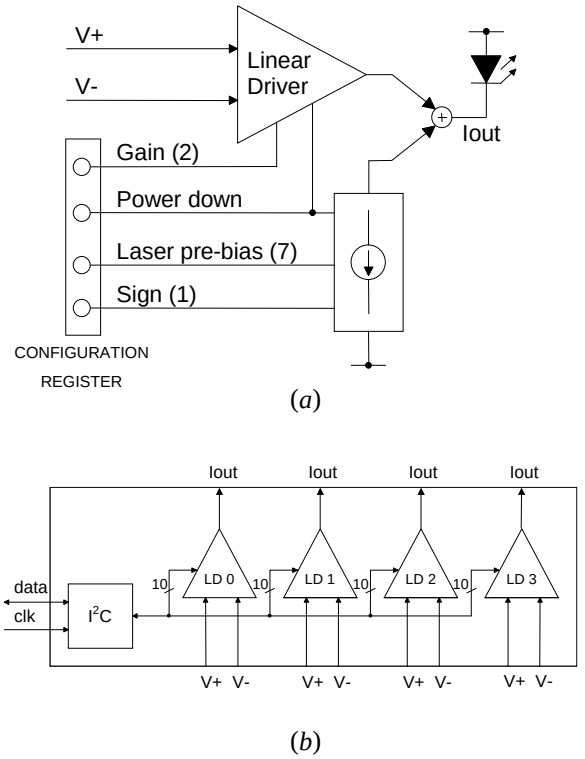

Figure 2: Linear Laser-Driver IC block diagram.

The channels can be individually addressed via a serial digital interface (I2C standard), which allows individual power down, gain control, and pre-bias control. The power-up configuration register is read from a set of hard-wired inputs. It is therefore possible to insure that the optical links are correctly biased at power-up.

The goal for the readout channel as a whole – from the Front End outputs to the digitising elements – is a performance equivalent to that of a 7-bit transmission system. The Linear Laser Driver should therefore exceed this specification. The following major specifications were set:

- Dynamic range: 8 bits
- Integral linearity: < 1% (over ±400mV)
- Eq. Input noise: < 0.8 mV
- Settling time: < 10 ns (to 1% of the final value)
- Bandwidth: > 100 MHz (at -3 dB)
- Cross-talk: < -60 dB

The IC should also have good power supply and common mode rejection, and be able to comply with a relatively large input common mode range (±250mV) while maintaining the linearity performance for 2.5V power supply.

III. CIRCUIT AND LAYOUT

The Linear Laser Driver consists of a Linear Driver and a pre-bias generator. The Linear Driver consists of a degenerate PMOS differential pair (Figure 3) and a push-pull output stage.

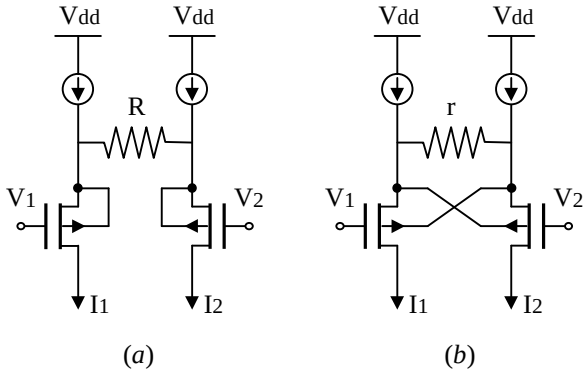

Figure 3: PMOS differential pair input stage, with parallel source degeneration resistor (a) and (b), and with cross-connected sources and bulks (b).

The differential pair, in comparison to alternative linearised design solutions, is conceptually simple and offers good dynamic and noise performance with limited power dissipation. The PMOS version is bulk-effect-free, thus allowing a larger input common-mode range. The required linearity can be obtained by two source-degeneration methods: a parallel source-degeneration resistor, and a source-bulk cross-connection between the transistors of the differential pair (as highlighted in Figure 3). The use of both methods (Figure 3-b) allows keeping the degeneration resistor to a value compatible with the required input common-mode range.

The push-pull output stage (Figure 4) is symmetrical and is thus compatible with the two modes of operation of the driver (source mode and sink mode). Two switched output stages can be activated in parallel, to provide four different selectable gains. In order to keep the power supply current constant, a dummy output stage dumps the complement of the modulation current directly into the power supplies (not shown in Figure).

The laser-diode pre-bias generator circuit consists of an array of current sources and sinks. The enabling logic allows them to be switched on and off as appropriate in order to generate a current linearly variable between –60 mA and 60 mA. A regulated cascode scheme [8] has been used to keep the output impedance high (>2-3kΩ, at ±60mA) and the compliance voltage low (<500mV) in all possible operating conditions.

To minimise the cross talk within a given chip, each individual channel contains its own independent bias circuit and power-down logic.

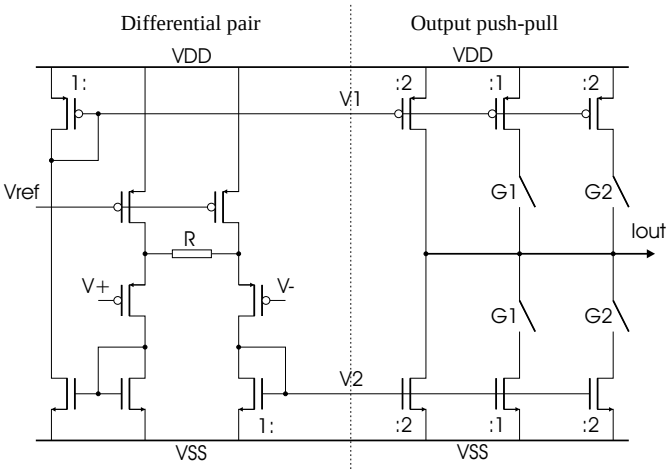

Figure 4: Linear Driver simplified schematic.

The circuit has been laid-out taking particular care of matching the differential pairs, the current mirrors, and the elementary current sources and sinks. All the NMOS transistors have enclosed geometry and isolation guard-rings to prevent the formation of radiation-induced leakage channels between source and drain in a same transistor or between adjacent transistors. These layout practices, together with the intrinsic good quality of the gate oxide of the technology being used, offer proven radiation tolerance up to levels which are compatible with the most stringent requirements of modern HEP experiments [9]. The Linear Laser Driver layout is shown in Figure 5.

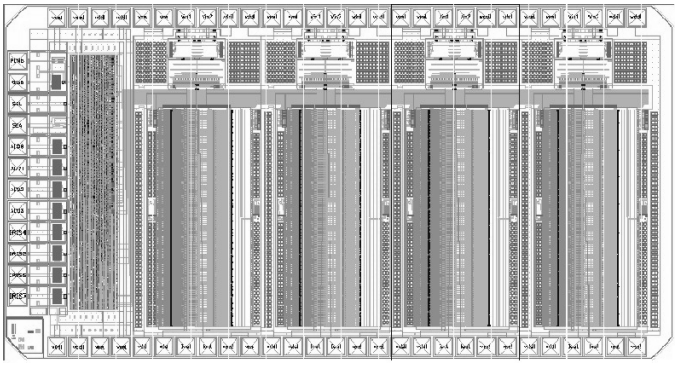

Figure 5: Linear Laser Driver layout (die size: 2mm x 3.75mm).

IV. Electrical Measurements

The Linear Laser Driver static, dynamic and noise performance has been tested extensively. Channel to channel variation within a single ASIC appears to be very limited.

The static performance of the devices has been measured with a Semiconductor Parameter Analyser, allowing to measure the output current on a low impedance, while the differential and common mode input voltages and/or output voltage are swept. Figure 6 shows the pre-bias current as a function of the programmed I2C register configuration (for a discussion of radiation effects, refer to Section VI). Figure 7 shows the static transfer characteristics of the LLD, for four different pre-settable transconductance gains. The measured gain values are 5.3mS, 7.7mS, 10.6mS, and 13.2mS.

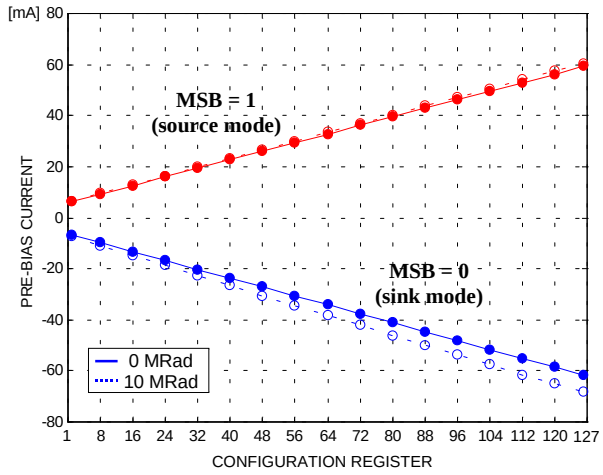

Figure 6: Pre-bias generation, in source and sink modes.

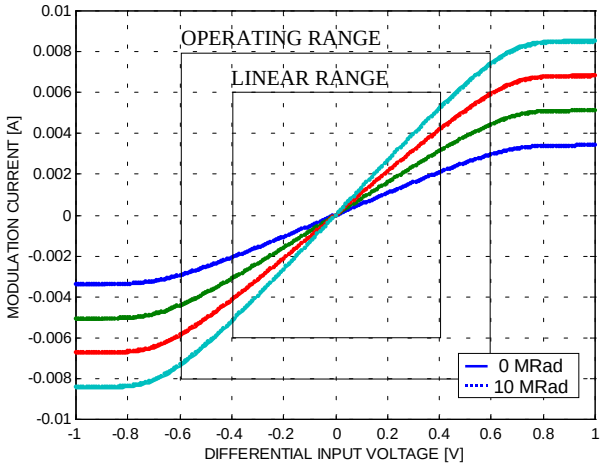

Figure 7: Static transfer characteristic.

Figure 8 shows the linearity error, for different input common mode voltages (Vcm = 0 and Vcm = ±500mV). The linearity error is calculated as the absolute difference between the real output current and its linear fit, and is expressed as a percentage of the specified operating range (*integral linearity deviation*). In absence of common mode, the error is less than 0.4% over the linear operating range. The common-mode has some impact on linearity, as shown in Figure 8. However, performance degradation is negligible for an output common mode between ±350mV. Figure 9 shows the integral linearity deviation as a function of the input common mode. In this plot, the improvement due to the active bulk configuration is visible and is quite significant for Vcm in the order of 500mV. For even higher common modes (and for both configurations) the ILD decreases again. This is however accompanied by gain degradation and overall dynamic range degradation.

The common mode rejection ratio is defined as the ratio between the common mode gain and the differential gain. This ratio is -40dB in the worst case (maximum pre-bias) and well below -60dB at low pre-biases.

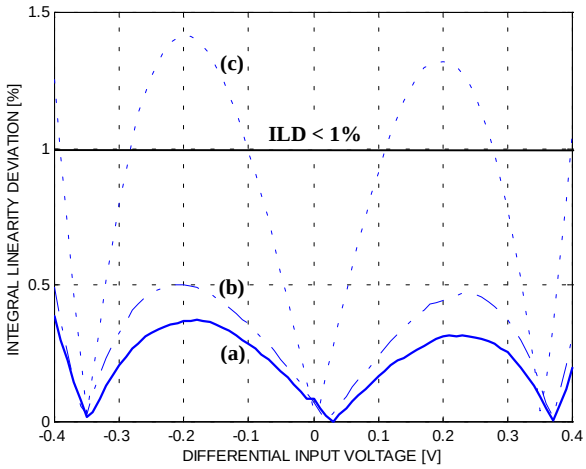

Figure 8: Linearity error for different input common modes: (a) Vcm= 0, (b) Vcm = -500mV, and (c) Vcm = 500mV.

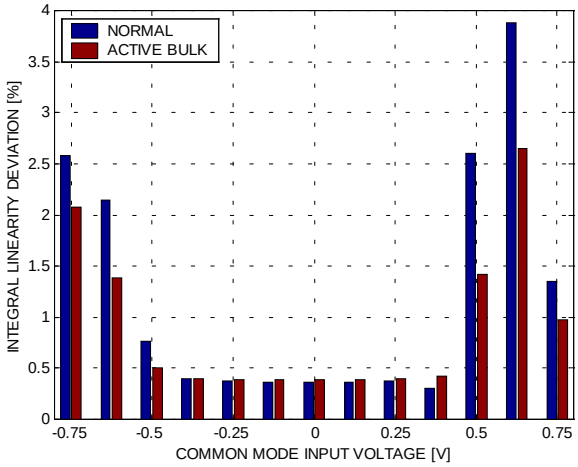

Figure 9: Common mode robustness for the normal and active bulk configurations.

The output impedance is of the order of 10kΩ at low pre-bias and decreases to 2-3kΩ at high pre-bias (the LLD output impedance is competing with the dynamic impedance of the laser diode, which is typically below 10Ω). The equivalent-input noise depends on the pre-bias and gain settings. It is proportional to the pre-bias and inversely proportional to the gain. The measured values vary between 0.4 and 1mV.

V. ELECTRO-OPTIC MEASUREMENTS

The LLD has been successfully integrated and tested in a CMS analogue optical link prototype [3], using optical transmitters and receivers which are representative of the final components. Figure 10 and Figure 11 show the optical link static transfer characteristics and noise characteristics, for the four LLD gains. The results are typical of a laser-based link. The LLD clips the input range at about 600mV (plots (a) and (b)). The photo-receiver being used clips the output range at 3.2V (plots (c) and (d)). The laser diode threshold clips the bottom of the operating range at around -500mV. The laser diode must be operated in the linear region of its characteristic (well above threshold). However, it is convenient to operate as close as possible to threshold, in order to: (a) limit power consumption, (b) profit of the reduced laser noise in this region (see Figure 11).

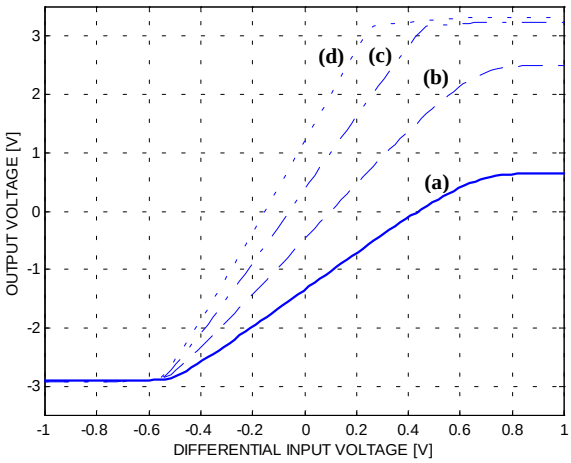

Figure 10: Optical link static transfer characteristic.

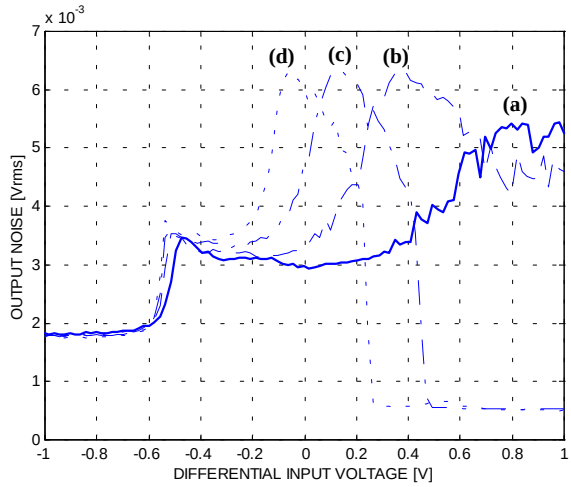

Figure 11: Optical link output noise characteristic.

The pulse response has been measured with input pulses of different widths and frequency. The step response exhibits very little overshoot and ringing (Figure 12), while the measured rise and fall times are below 4.5ns. The measured settling times (to within 1% of the final value) are about 15ns. The -3dB bandwidth has been measured with a network analyser and is found to be ~110MHz. Cross-talk between channels is below 0.3%.

The measured power consumption is of the order of 33mW per channel at minimum pre-bias and minimum gain. The power consumption increases proportionally to the pre-bias current and is also to some extent dependent on the gain and on the operation mode (source or sink). The maximum power consumption is below 185mW.

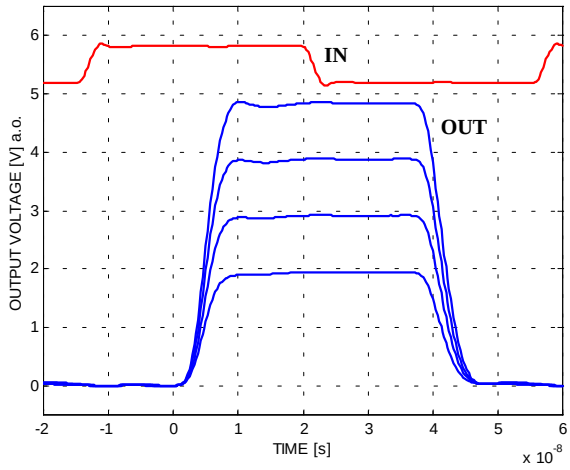

Figure 12: Optical link pulse response.

VI. Radiation Testing

The circuit has been tested for total ionising dose effects using a 40kV X-ray source, to investigate possible performance degradation related to ionising effects (charge trapping in oxide interface states). The experiment has been carried out according to ESA/SCC recommendation for IC qualification with respect to total dose effects [10]. The chip has been irradiated in two steps to 1Mrad and 10Mrad (SiO_2), at a constant dose rate of 21.2Krad/min. After irradiation the chip was annealed for 24 hours at room temperature, followed by 168 hours at 100°C (accelerated life). The full set of static and dynamic measurements was carried out after each step in order to assess any change in performance. The chip was under nominal bias during irradiation with the four channels switched on (two of them operating at maximum pre-bias and two at minimum pre-bias).

The results of radiation and accelerated life testing show that the LLD will operate within specifications all during the experiment lifetime (10 years). The overall radiation effects are negligible or acceptable. The pre-bias source current is stable, whereas the pre-bias sink current shows an increase of 10% (visible in Figure 6). This is attributed to the NMOS type V_T-referred current reference and is compatible with the previously measured threshold variations in NMOS devices [4]. There is no significant change in the LLD static transfer characteristics (in Figure 7 the pre- and post-irradiation plots match almost perfectly) and dynamic characteristics.

VII. Conclusion

A Linear Laser Driver array has been developed and implemented in a 0.25µm CMOS technology. The device has been designed to comply with the CMS requirements for analogue optical transmission in the Tracker readout. It is however also compatible with digital optical transmission modes in the Tracker slow control system. Sample devices have been tested and shown to be fully functional. The switched gains can be used to equalise the significant insertion loss spread expected from the 50 000 analogue optical links. The pre-bias current is programmable over a wide range, with 7bits resolution, allowing tracking of optical source degradation during detector lifetime. The LLD array has a modularity of four channels. However, since the channels can be individually disabled any modularity below that can also be chosen without a power penalty. The extensive set of measurements showed that the device matches or exceeds the required analogue performance. Integral linearity deviation is better than 0.5% over an input common mode range of ±350mV. Input referred noise is less than 1mV in an analogue bandwidth of 110MHz. Power dissipation at maximum pre-bias is below 200mW per channel. The radiation testing of one device showed that the analogue performance would also be maintained after a total ionising dose comparable with the one expected during the experiment lifetime.

VIII. References

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