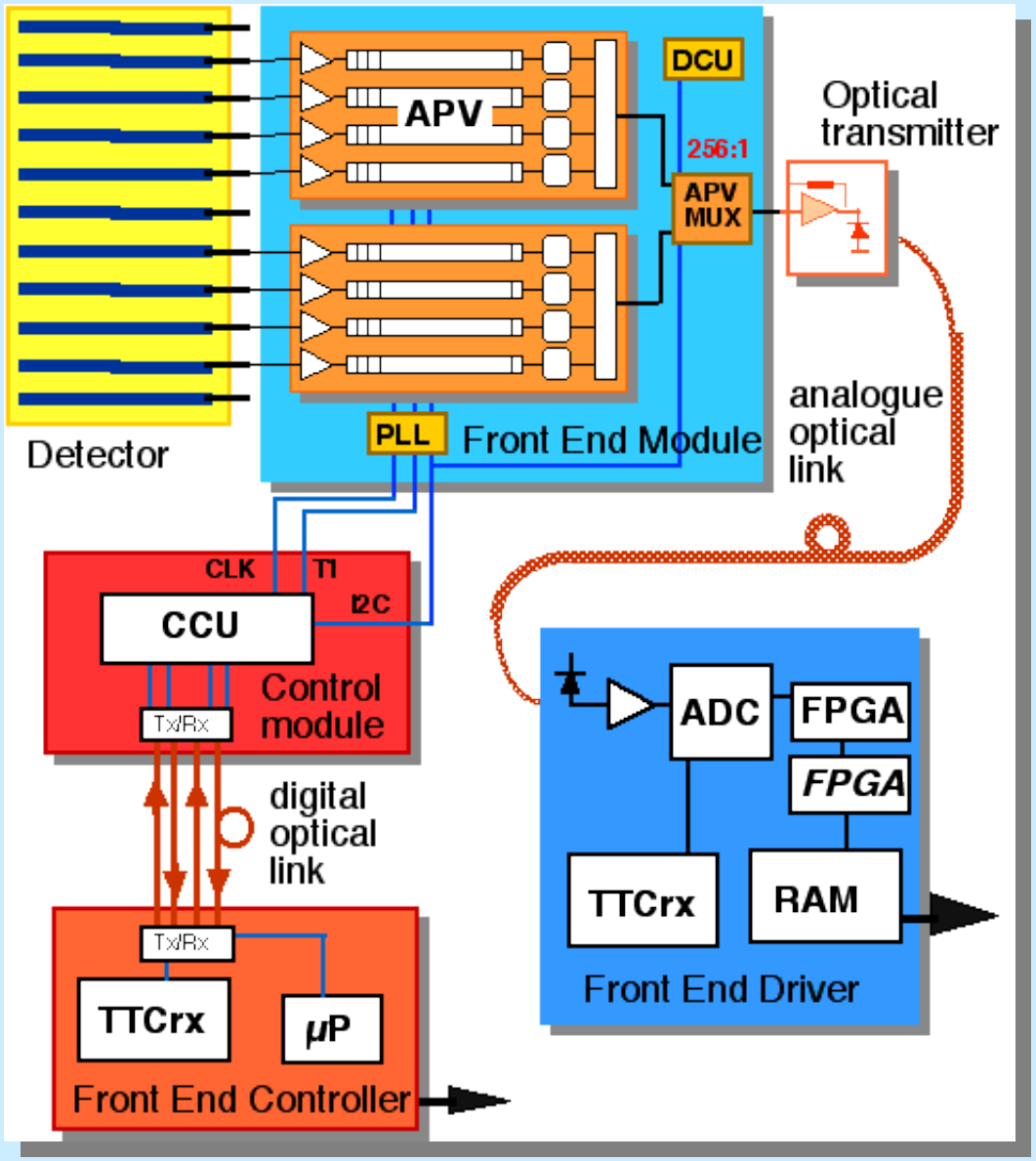
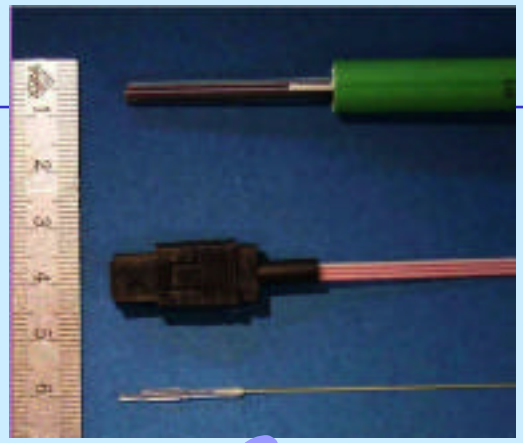
CMS microstrip tracker readout

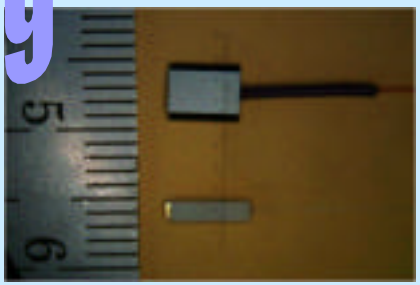


- Front end *almost complete*
  APV25 frozen
  final DCU, MUXPLL submitted
  0.25µm contracts in place
- Optical link *very advanced state*
  ready to start procurement
- DAQ interface *PMC FED exists*
  final FED being designed
- Control system *well advanced*
  FEC & 0.25µm chip set exist
- System
  under construction in CERN lab
  25nsec beam May 2000

Optical link status



1999



- Project entering production phase
- Feasibility demonstrated with close to final components
- Robustness & radiation tolerance measured
- Market surveys for all elements in the chain
- Manufacturers of lasers and connectors short-listed
- Final calls for tender needed mid 2001

Final system and costs depend on tender actions

NB non-trivial to manage these large tenders

interdependent components, booming electronic market, special requirements, small volumes cf commercial demand

2000

Why analogue optical link PRR now?

- Optical link components well factorised from remainder of readout system

  but tightly linked in finalising system

  Exhaustive scrutiny of component performance (& manufacturers)

  final components (and costs) needed (ESR) but...

  ...can't procure pre-production components without completion of tenders

  some system elements (eg FED) can't be finished without final optical links

  final FED now essential for large scale acceptance tests from 2002

- Now need to make commitments

  Commercial procurement on large scale (for HEP)

- This talk - snapshot of system

  Main missing information

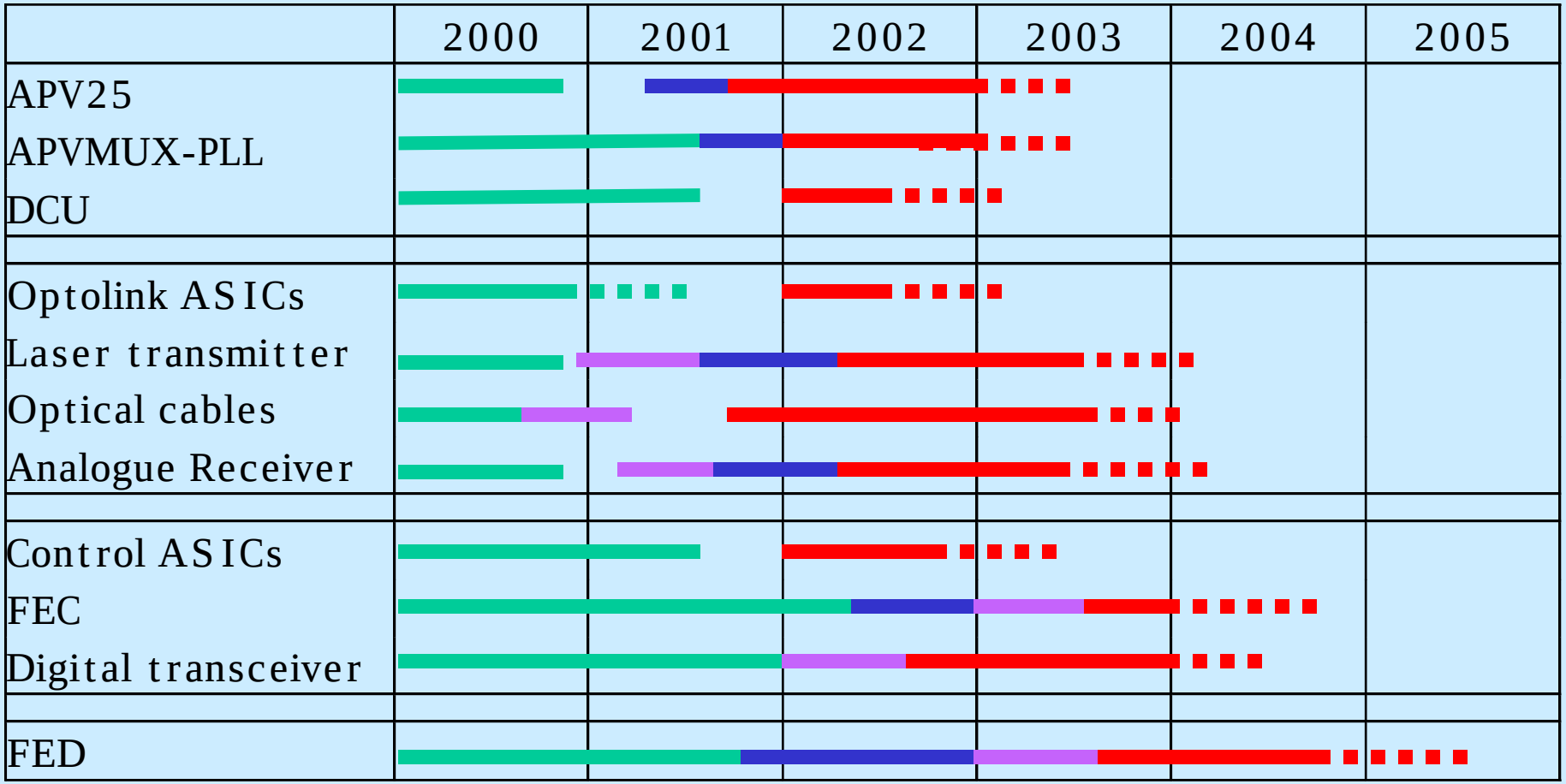
  system tests with modules in realistic mechanical & electrical environment

- Glossary (offline) please see

  http://pcvlsi5.cern.ch/CMSTControl/documents/GeneralDoc.htm

  Readable system summary + references to considerable published information

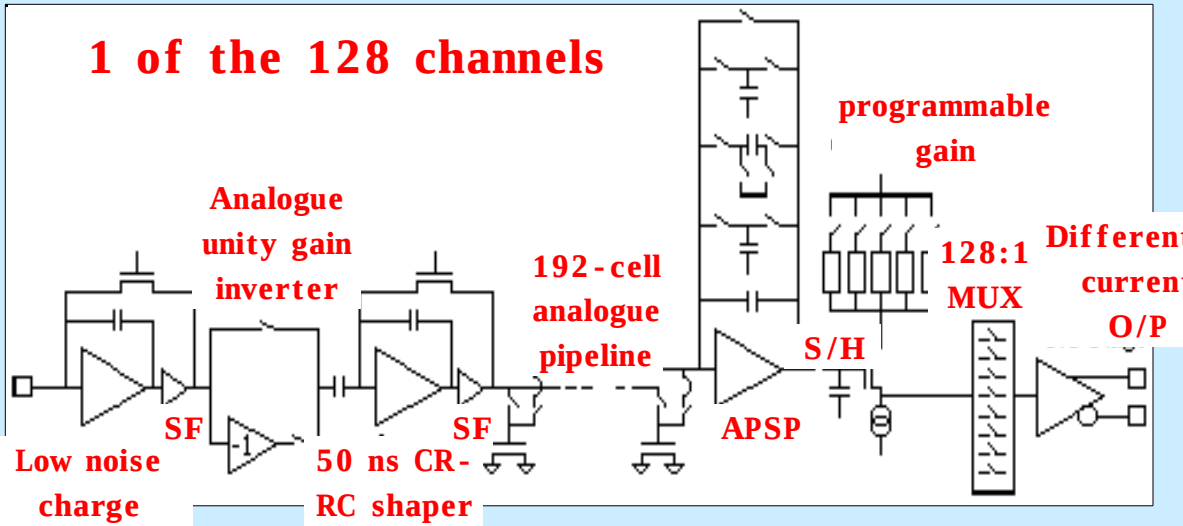
Major components and schedule

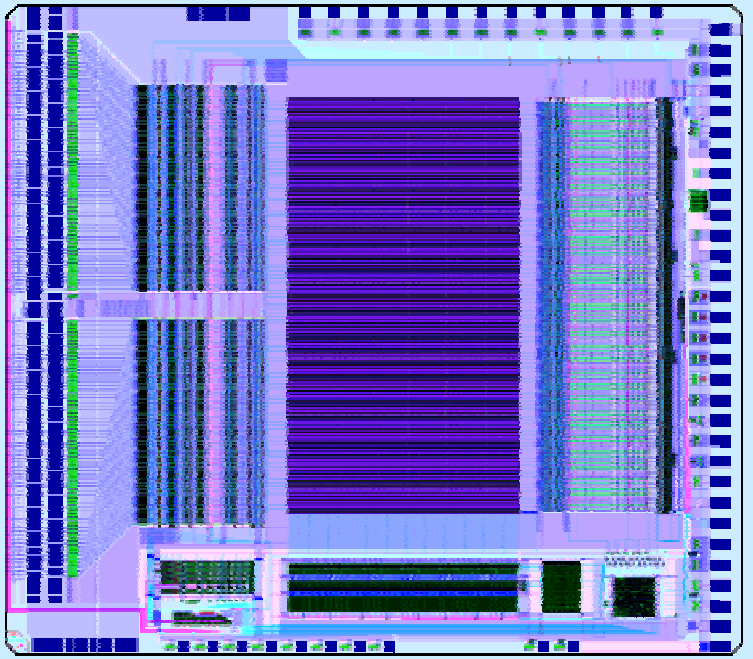


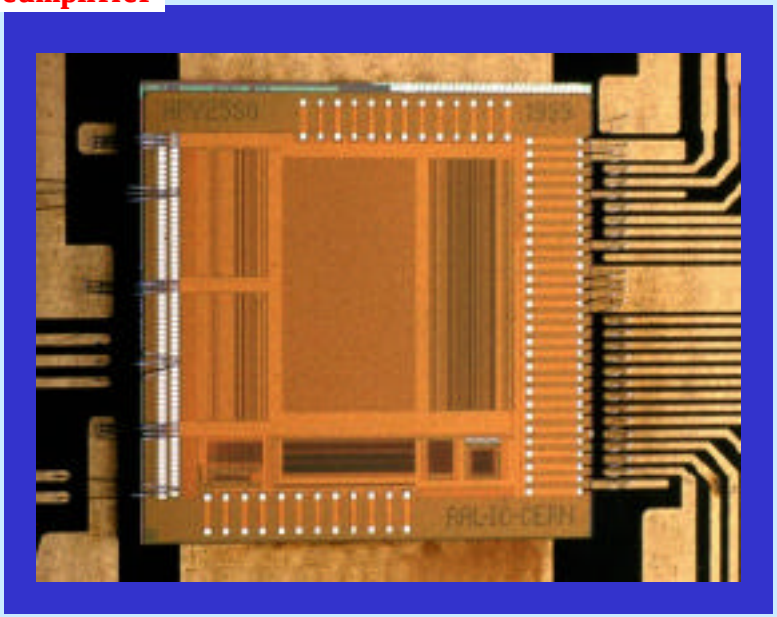
NB budget profiles still influence !

FEC & FED development modules exist for module & system tests

APV25 0.25µm CMOS







APV25-S0 (Oct 1999)

Chip Size 7.2 x 6.5 mm

APV25-S1 (Aug 2000)

Chip Size 7.1 x 8.1 mm

Final

New features in 0.25µm APV

- **Motive for late change of technology**

  Radiation hardness from standard reliable process & significant cost gains

- Strategy

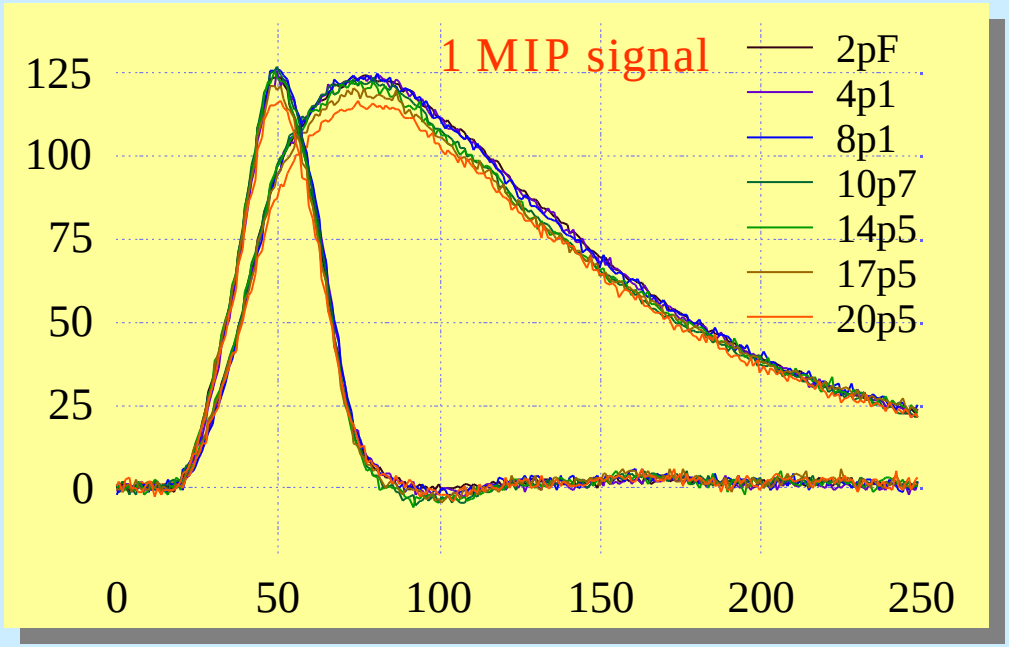
  only changes essential for new process *e.g. 2.5V power supply*

  + few system level enhancements - e.g.

• Longer pipeline	192	*[160]*
• Deeper buffers	10 (x3)	*[6 (x3)]*
• S/N improved	2000/0.36 PMOS @ 400µA	*[3000/1.4 PMOS @ 500µA]*
• Switchable input polarity & differential output		
• Reduced size	57mm^2	*[77mm^2]*
• Reduced power	2.3mW/channel	*[2.4 + MUX]*

- **All benefits realised**... entire system based on single 0.25µm process

Typical lab test results APV25-S1



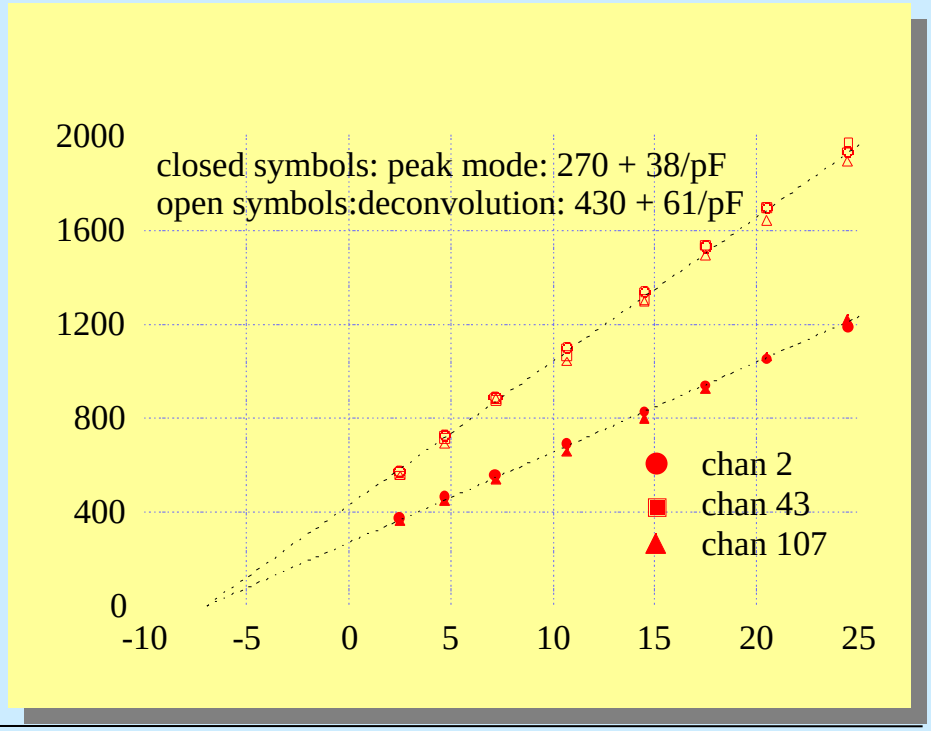
- System specification

  Noise <2000 electrons

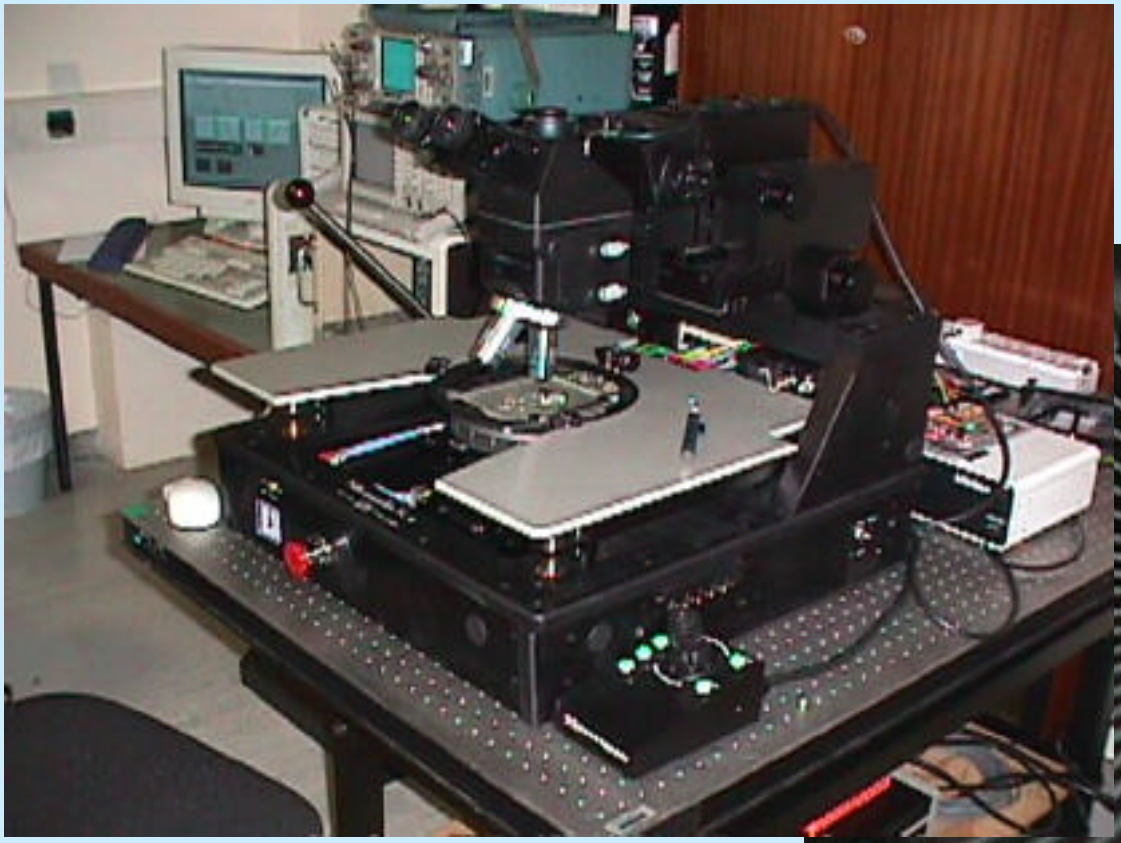
  for CMS lifetime

- < 5 % non-linearity to 5 MIPs
- Pipeline pedestals & gain uniformity

  additional noise typical < 150e
- Significant speed & V_{supply} margins
- Good noise uniformity

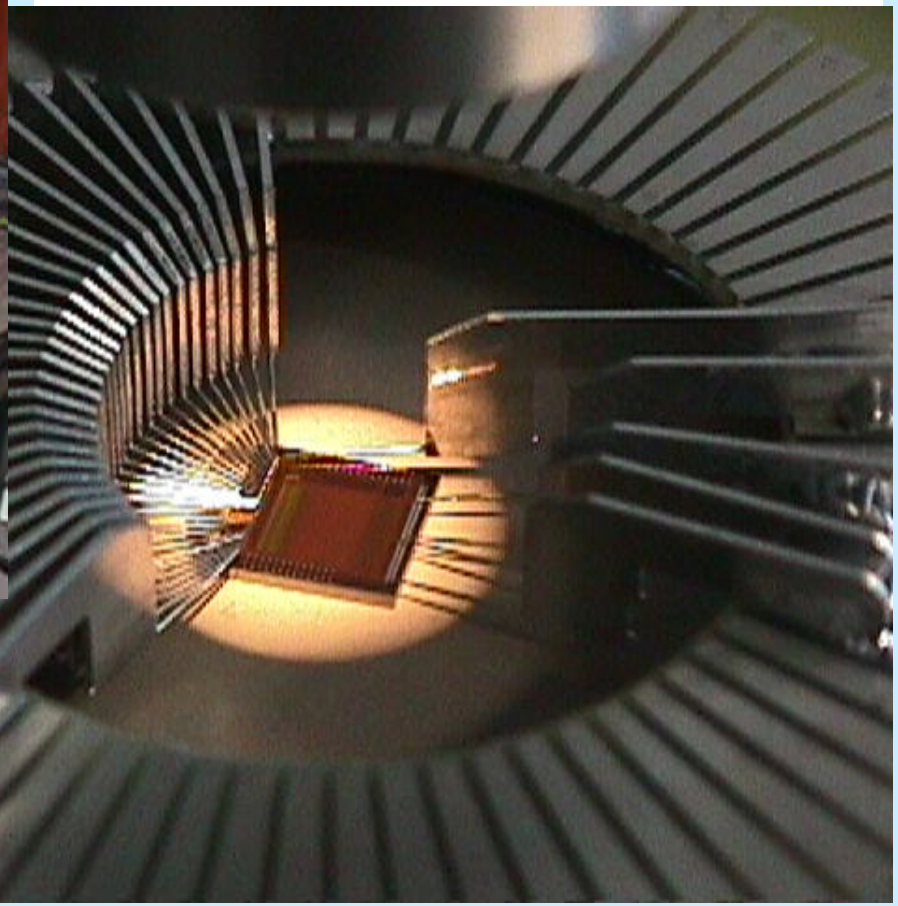


Chip testing



- Automated on-wafer testing

  experience from cut APV25 die



- Operational at Imperial College

  Second set-up at RAL

Chip testing summary

to be used in production

- **Digital functionality**
- **Power supply currents**
- **Analogue tests**
  - Every channel
  - Every pipeline location
    - *only noise not measured*
    - *on-wafer*

Basic digital functionality
I2C functionality (read/write to all locations, test for stuck bits, response to all possible chip addresses) Check for correct address in digital header Look for header error bit set after 1000 pseudo-random triggers
Power supply currents
Verify VDD and VSS currents within acceptable range
Pipeline
Measure pedestals for every pipeline cell for all channels, look for bad locations (high/low pedestals) and correct pipeline column address in header
Channel pedestals
Verify analogue baseline can be adjusted and measure pedestals, look for high/low channels. Do this in both peak and deconvolution modes.
Channel calibration
Measure pulse shape for all channels in peak and deconvolution modes. Look for bad channels (low pulse heights).

- **Test time < 2mins/chip**
  - => *1 8inch wafer per probe station per day*
  - => *Complete testing in ~1 year*

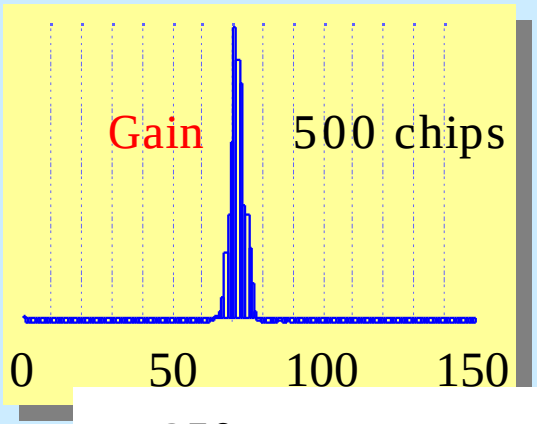
APV25 chip testing results

- Consistent high quality from MPW and 10 wafer order

  APV25-S0 passed all tests: 84% (500 die)

  APV25-S1 cut wafer yield : 66% (~222 die)

  Uniformity excellent



- 8 inch APV25-S1 wafer testing under way

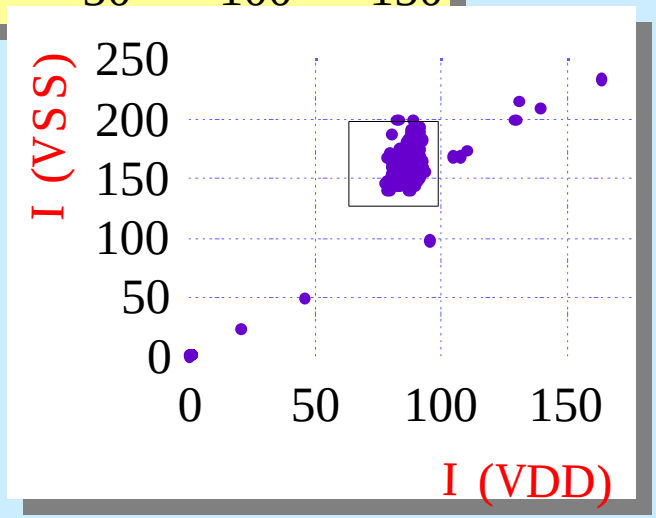
  3/9 wafers tested to date

  refining final tests, criteria & software

  Data base prepared

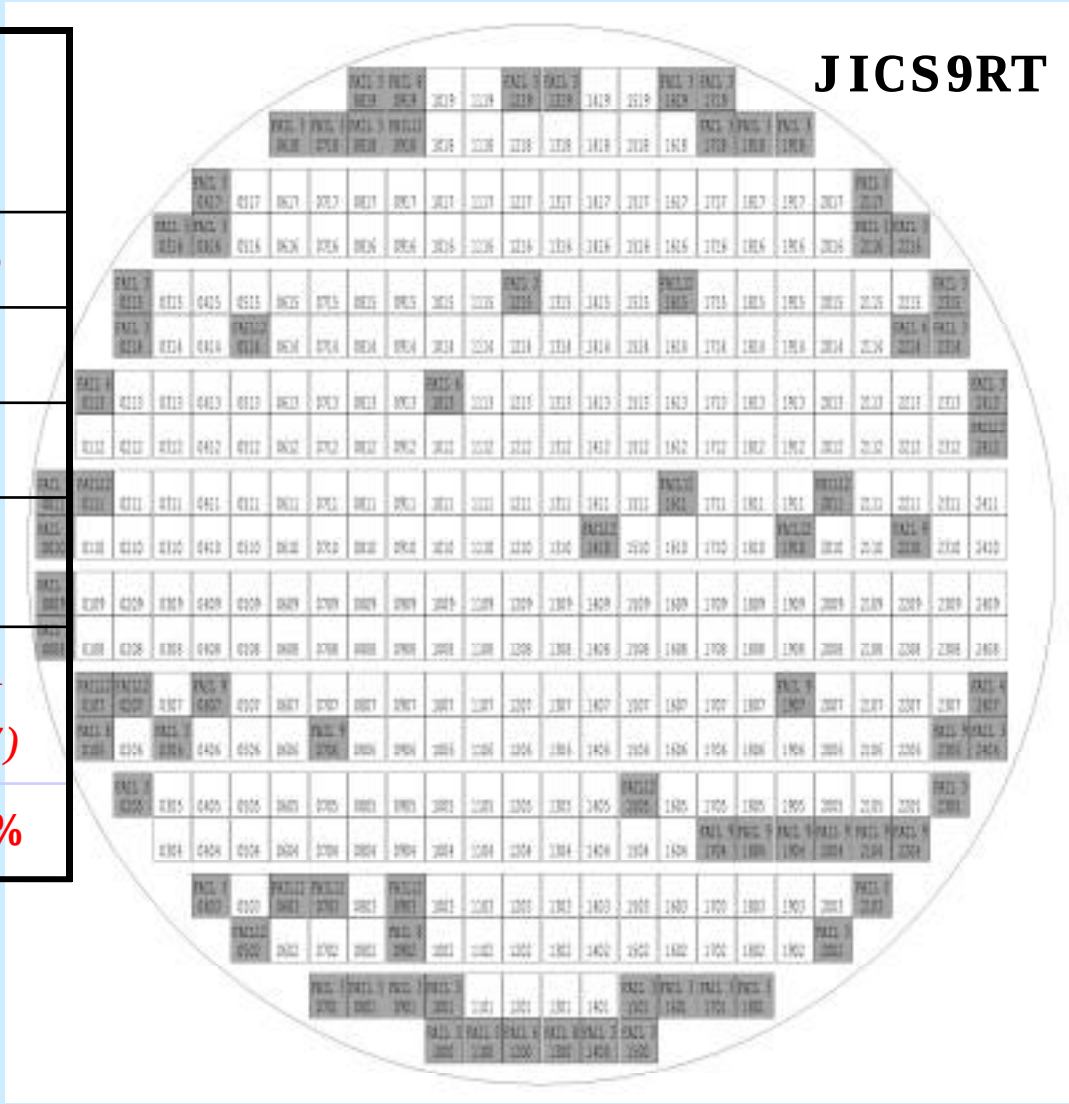
  Do not expect problems to match module production schedule

  draft QA document exists (for all chips)



APV25 wafer test results

	JLCS9NT	J0CSEPT	JICS9RT	Total Fails
Digital	68	52	48	168
Power	4	6	3	13
Pipeline	9	6	8	23
Channels & calibr.	36	26	25	87
Total *(edge)*	117 *(60)*	90 *(49)*	84 *(48)*	291 *(157)*
Yield	**70 %**	**77 %**	**79 %**	**75 %**

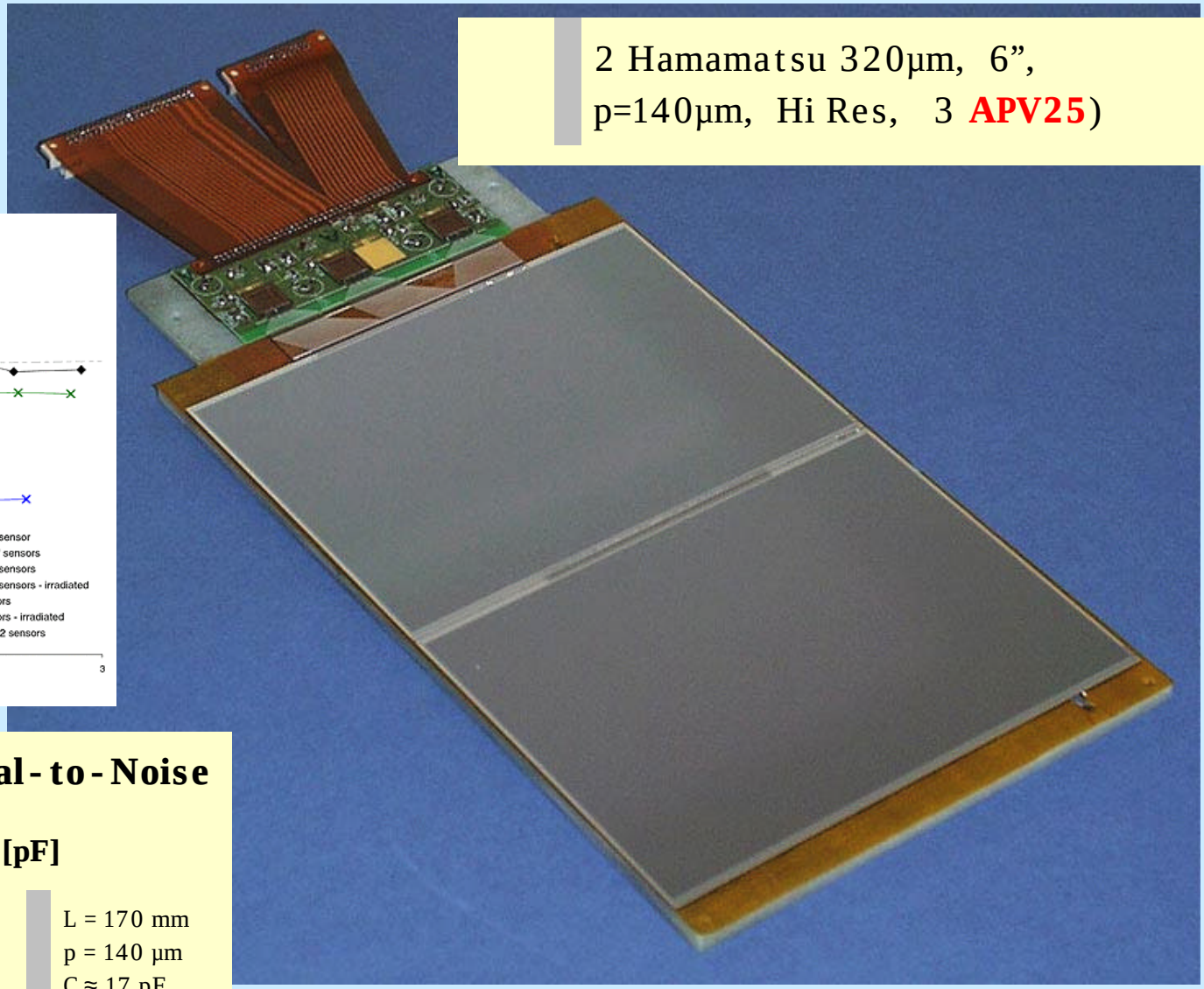


- Cut wafer **retest**

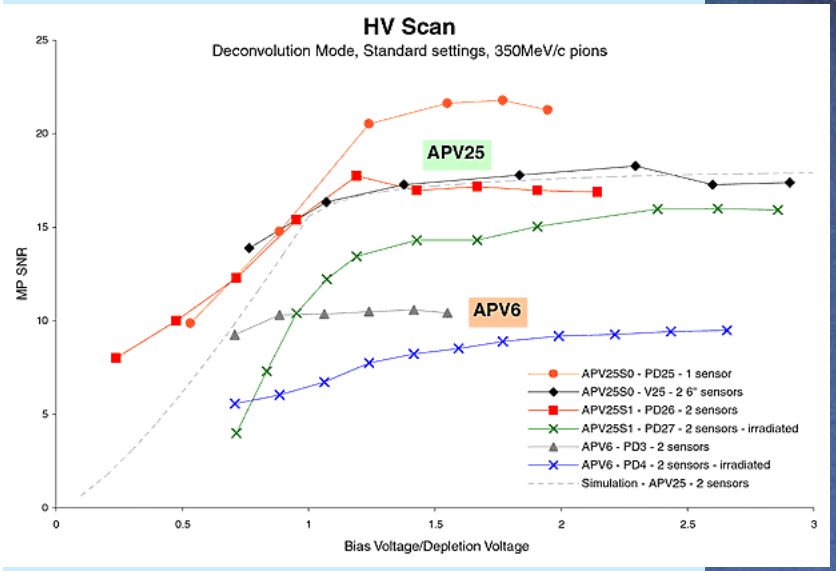
  wafer cut poor quality but

  still <2% good die failed

300 MeV/c π beam test (Vienna)



2 Hamamatsu 320µm, 6”,
p=140µm, Hi Res, 3 **APV25**)



APV25	**Deconvolution Signal-to-Noise**		
predict	**ENC [e] = 430 + 61 / [pF]**		
Vienna	**SNR (meas.)**	**17**	L = 170 mm
3 APV25	SNR (predict)	17.0	p = 140 µm C ≈ 17 pF

Irradiations of 0.25µm technology

- Much pre-existing data

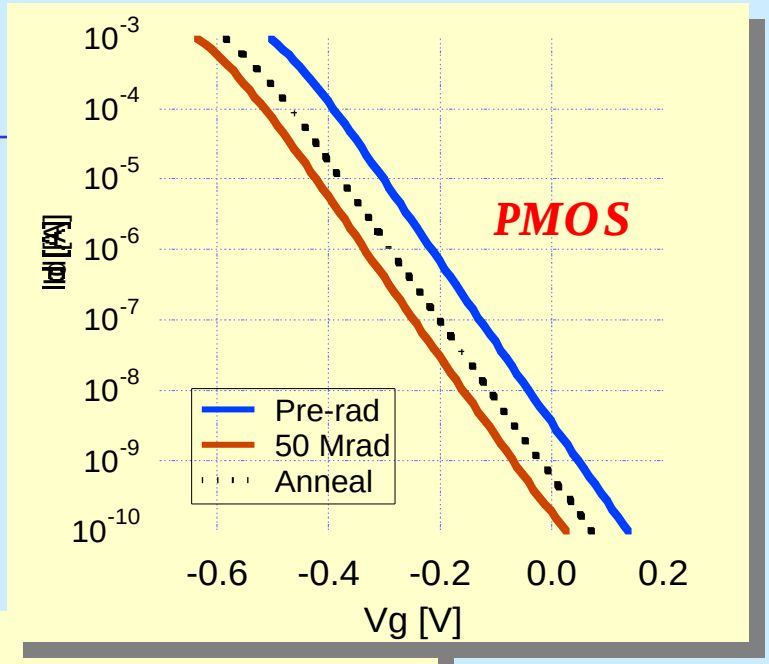
  Extensive RD49 studies

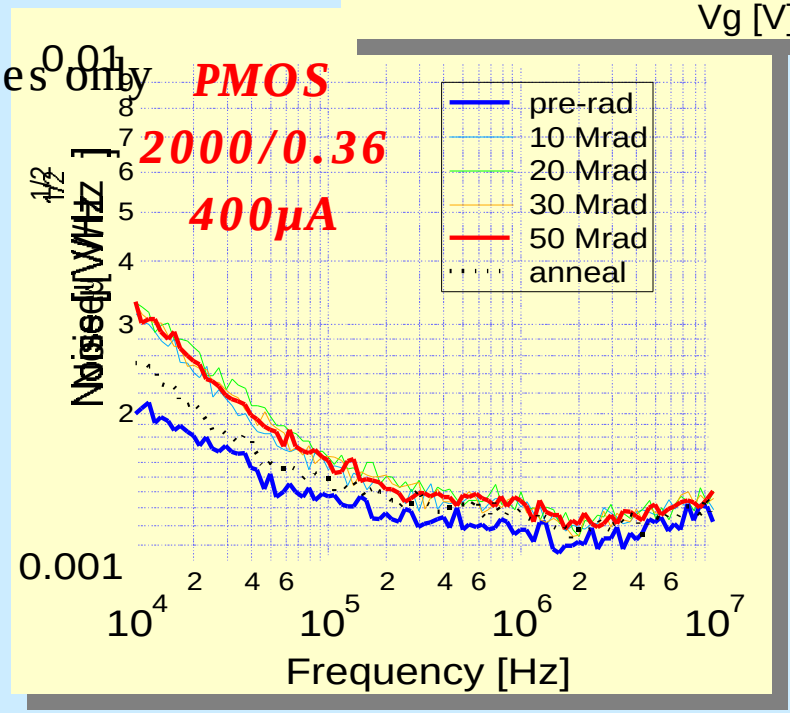
  CMS tracker data from IC, Padova, CERN

  ALL POSITIVE and well beyond LHC range

- CMOS hard against bulk damage

  Can be qualified with ionising sources only





- Typical irradiation conditions

  50kV X-ray source

  Dose rate ~ 0.5Mrad/Hour

  to 10, 20, 30 & 50Mrad

  dosimetry: Si diode ~10% precision

  Anneal: 1 week at 100°C

APV25 irradiations (IC & Padova)

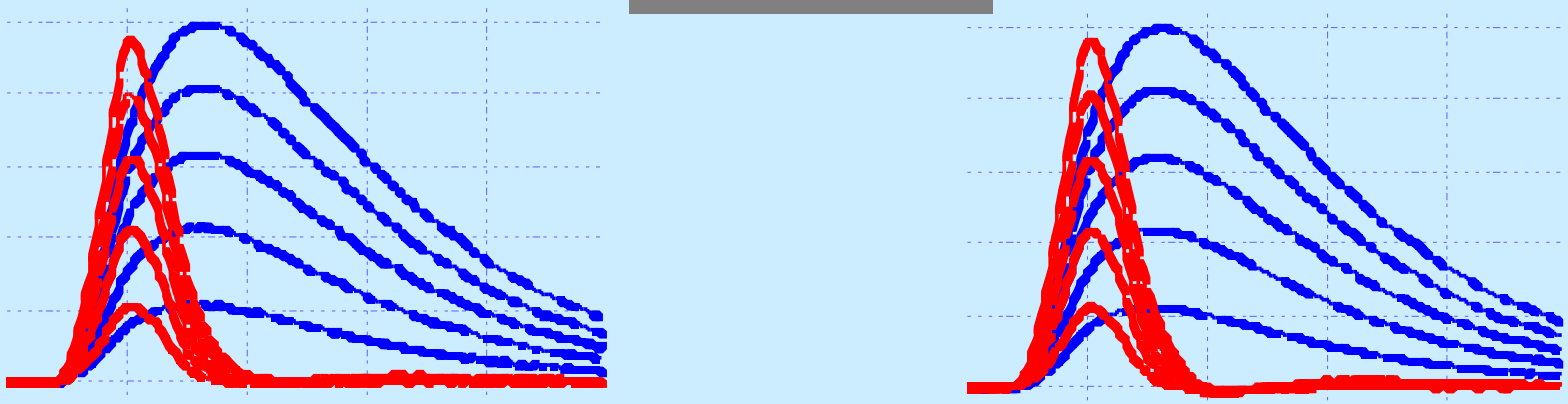
- IC x-ray source

  Normal operational bias during irradiation clocked & triggered

Post irradiation noise change insignificant

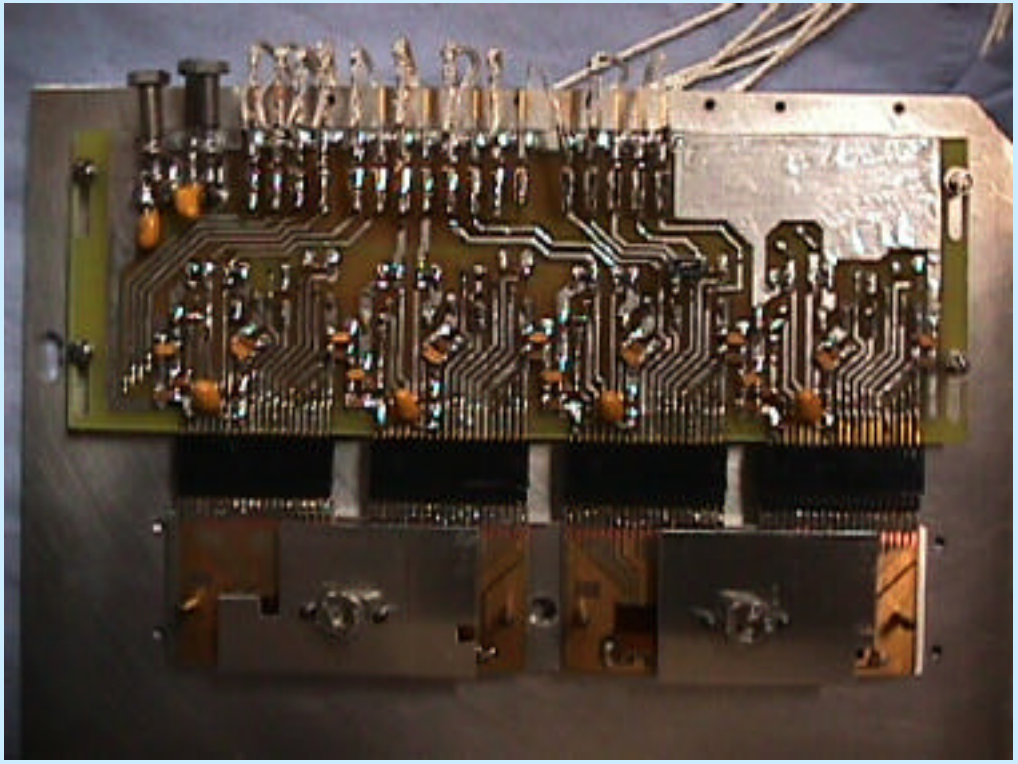
APV25-S1

pre-rad **10 Mrad**



also 10 MeV linac electrons(80Mrad) and 2.1x10^{14} reactor n.cm^{-2}

Single Event Upset tests Heavy ions and pions



Ion	Si	Cl	Ti	Ni	Br	I
LET ($MeV.cm^2.mg^{-1}$)	9 - 10	13 - 16	20 - 23	28 - 32	39	62

- local highly ionising particle near sensitive circuit node can change state of logic elements

  origin - knock-on silicon ions in chip

- 4 APV25s in three tests

  Feb 2000, July 2000, Dec 2000

- Measured circuit cross-sections

  include in CMS Simulations

- *Conclusions* - full system

  ~150 SEU per hour

  = 0.15% APV25s

  verified in π beam Dec 2000

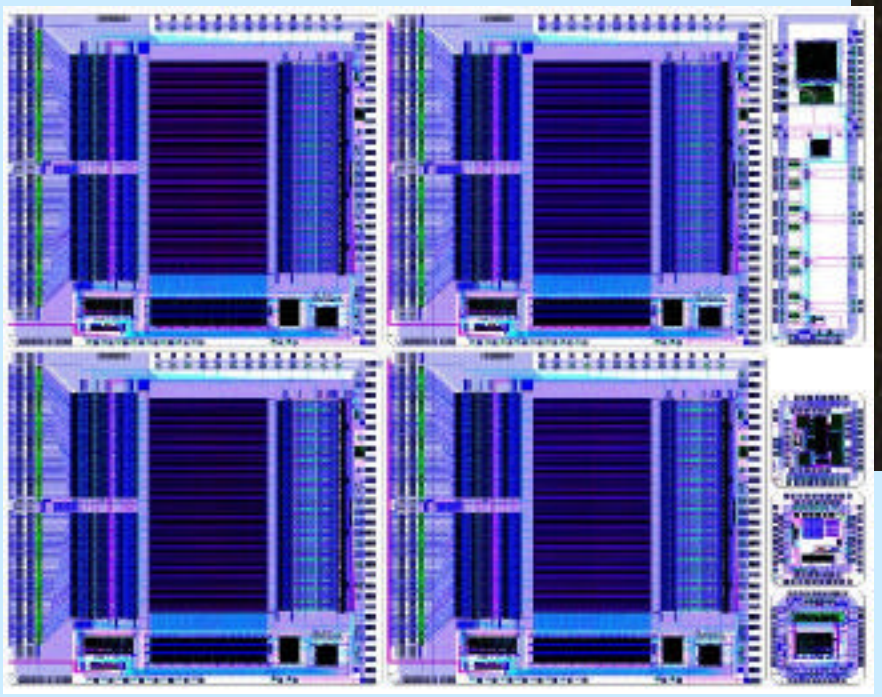
  Technology very robust

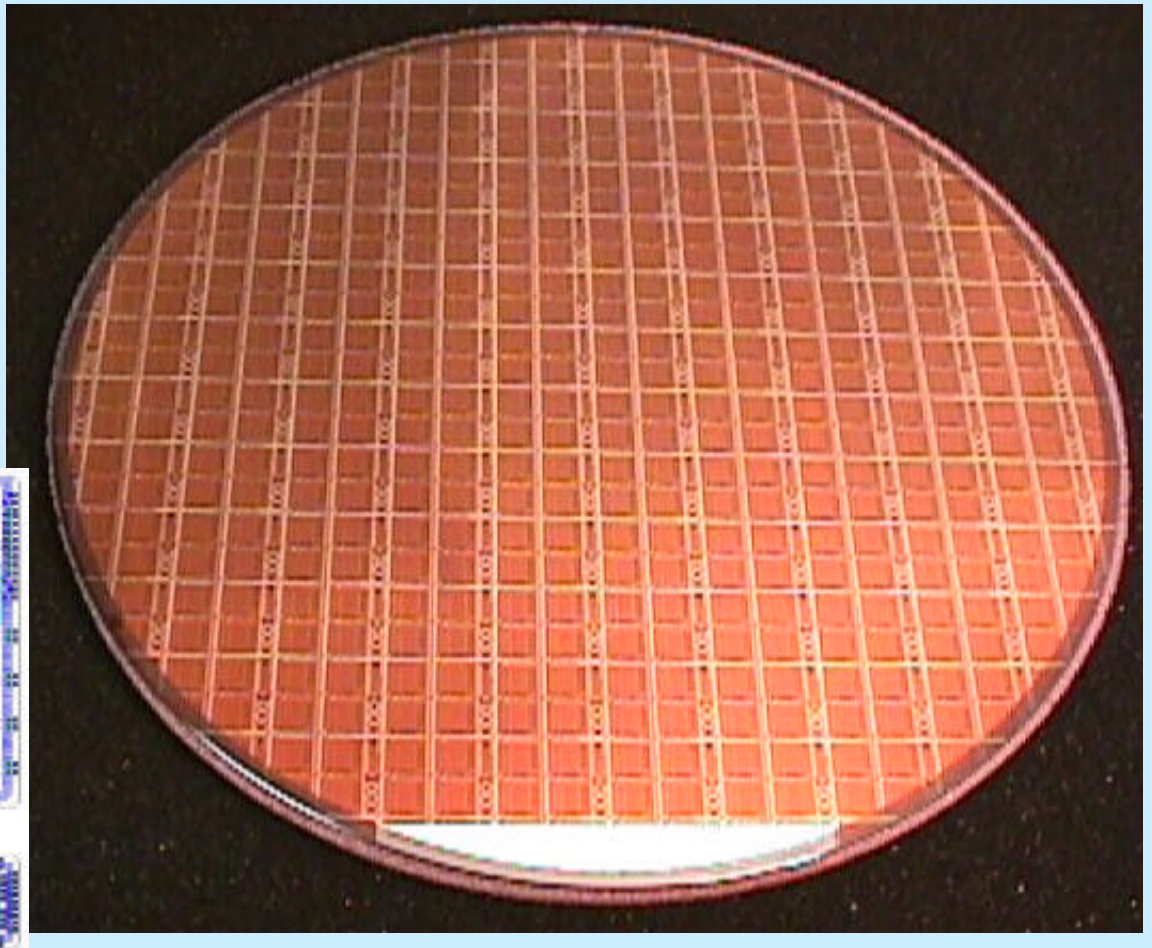
Production wafer layout

- Overall size 200mm
- APV25 die ≈ 400
- APVMUX+PLL die ≈ 100

Reticle dimensions

18,420mm x 14,400mm





Other FE chips (i) APVMUX-PLL

- to ease production, FE PLL + APVMUX as single chip

  electrically independent

- PLL guarantees good clock & T1 on module

  + *fine tuning of delay*

  individual version successfully tested

- APVMUX interleaves 4x2 APV 20MHz data streams

  => *transmission switch*

  die delivered August… problem on test - extra power

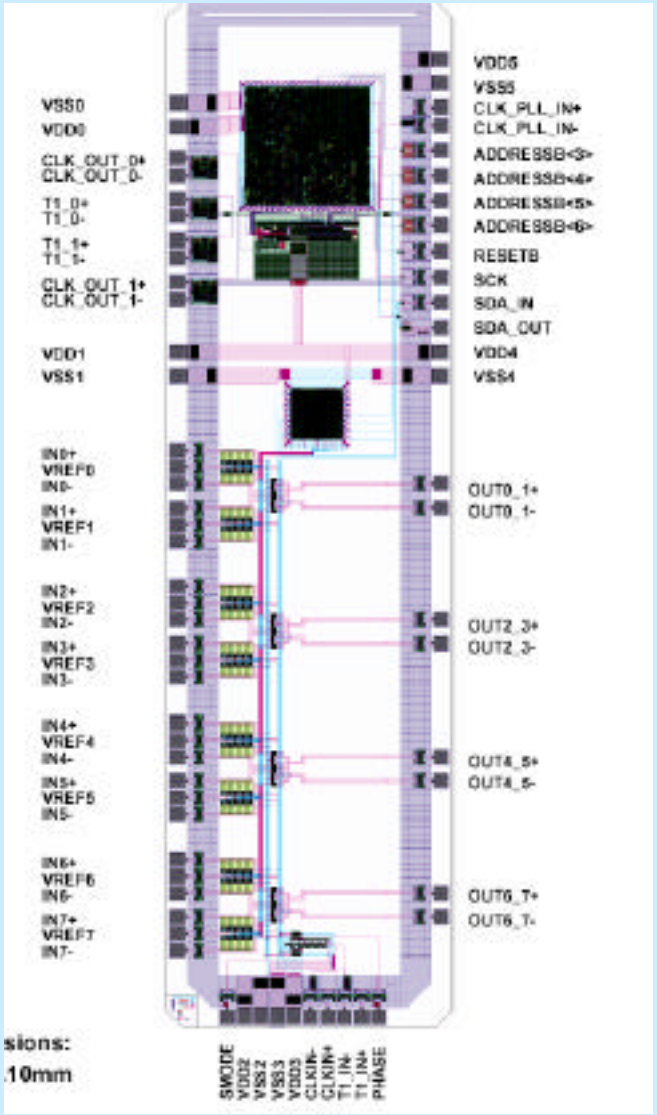
- Resubmitted October MPW run (-> March 2001)

  single mask layer change to correct fault

  further minor fault - resubmit May 2001

- Main impact now on schedule

  need to finalise FE hybrid



FE hybrid (Strasbourg)

- Ceramic hybrid

  Choice of technology Oct 2000

- First TIB hybrid - Nov 2000

  CERN workshop manufacture

  PLL-MUX problem complicates operation

  problem with 30mΩ resistance

  solved + ...

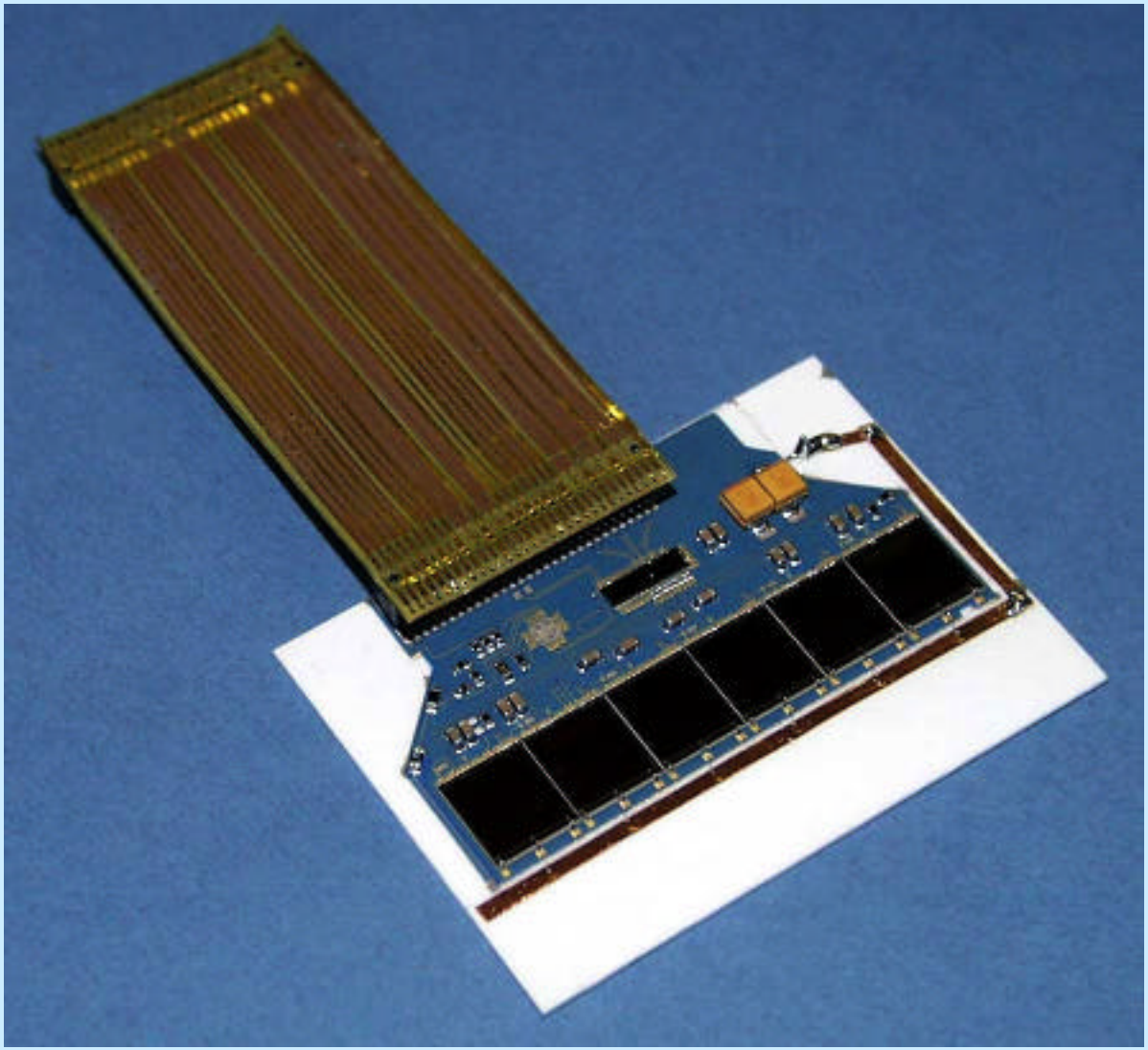
  ... *robust at system level*

- TOB hybrid delivered April 2001

  to deliver system test

- Industrial production foreseen

  Market survey beginning



Hybrid test in Vienna Feb 2001

- Readout system as used in beam and SEU tests

System: 6 APV25 + APVMUX → 3 analog channels

IntCal: 1 MIP level (ICAL=36)

Typical IntCal Signal and Noise values

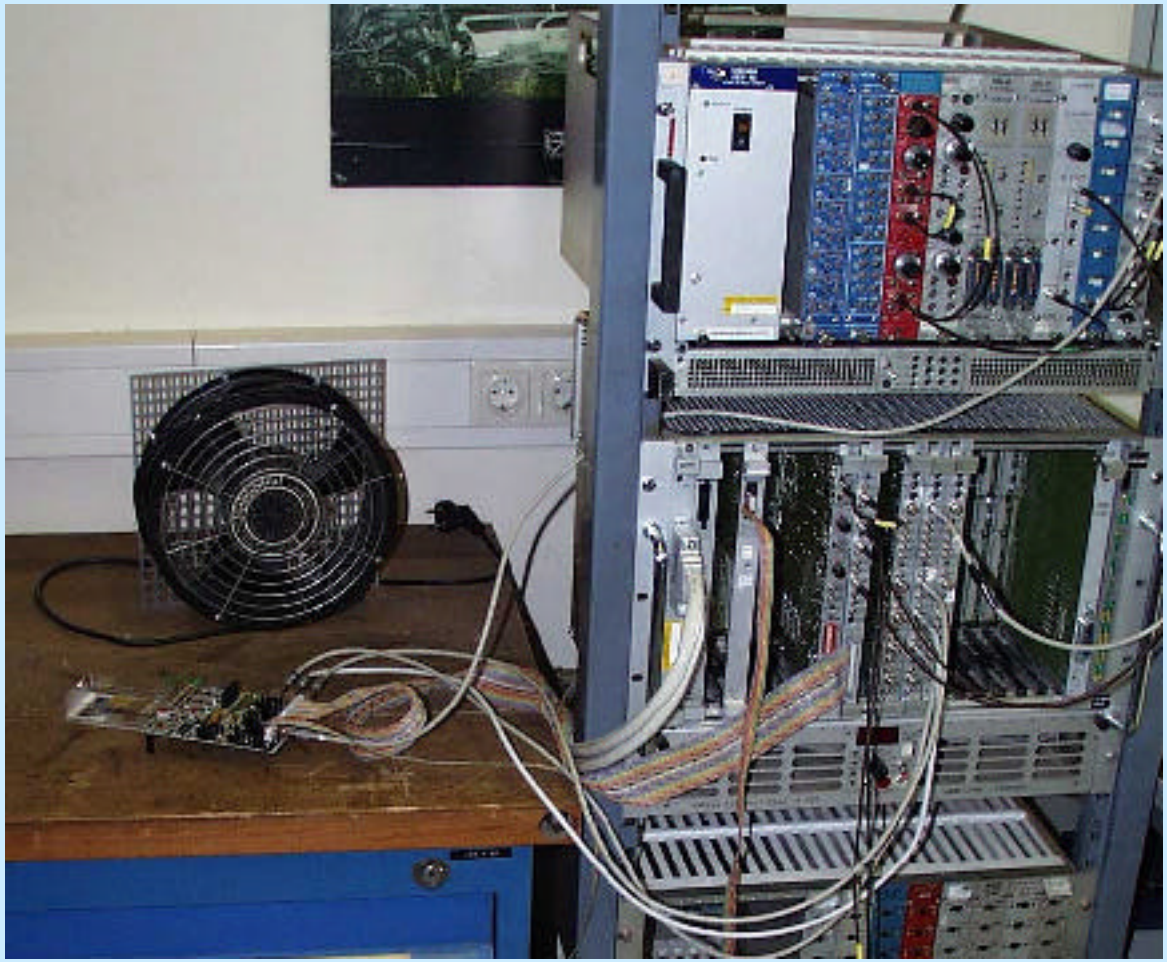
Noise [e] is calculated assuming 22500 e from ICAL=36

(no detector)

Mode	Signal [ADC]	Noise [ADC]	SNR	Noise [e]
Peak	72	1.10	65.5	344
Deconvolution	83	1.58	52.5	428

Dec Noise: **ENC [e] = 400 + 60 / [pF]**

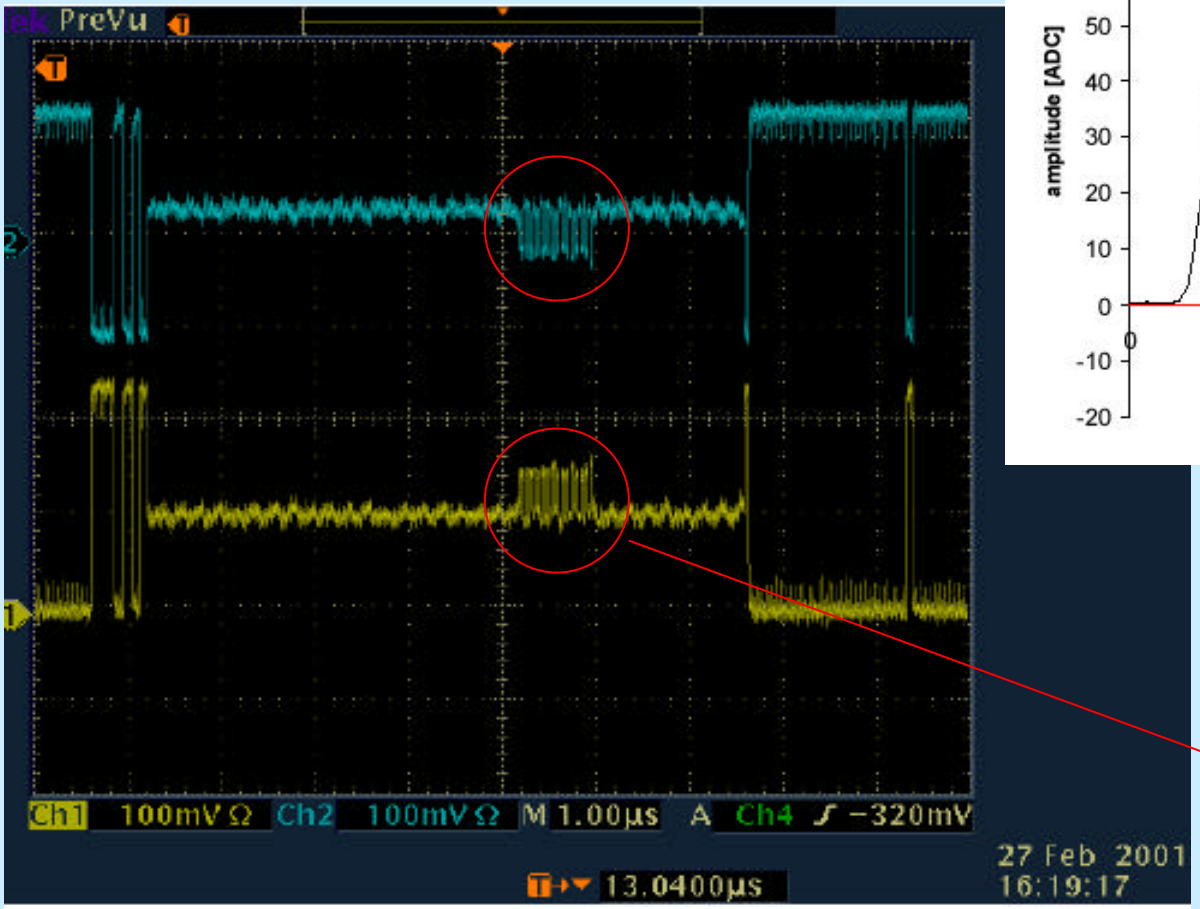
good agreement

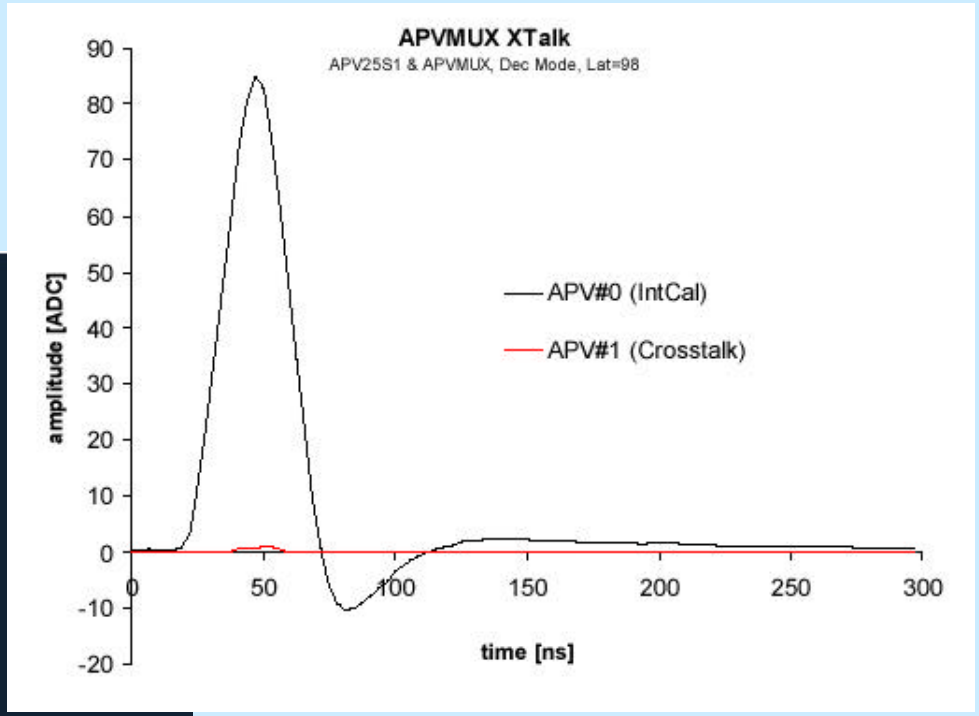


APVMUX performance on hybrid

Draws current, yet works perfectly

Xtalk test — IntCal on even APV, nothing on odd





Xtalk — virtually nothing

MUX switch — 3 ns risetime

differential output
calibrate on 1 APV

Other FE chips (ii) DCU

- Current, temperature and V_{supply} monitoring

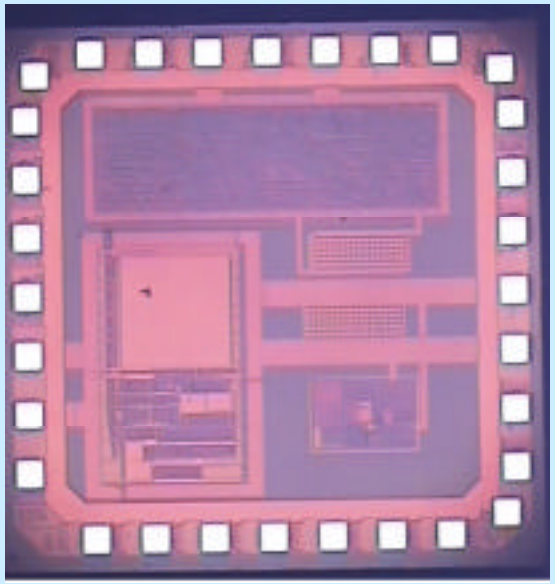
  Specifications & footprint frozen

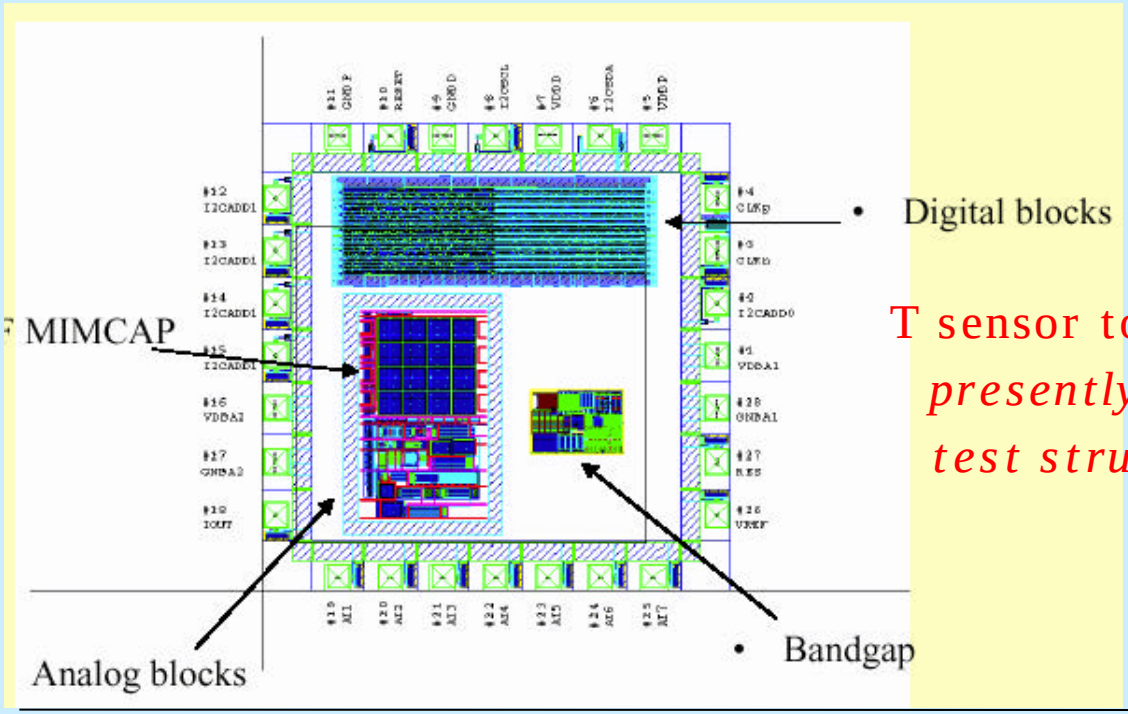
  chip fabricated, first iteration problem

  second version meets requirements

  possible fine tuning

- Freeze summer 2001

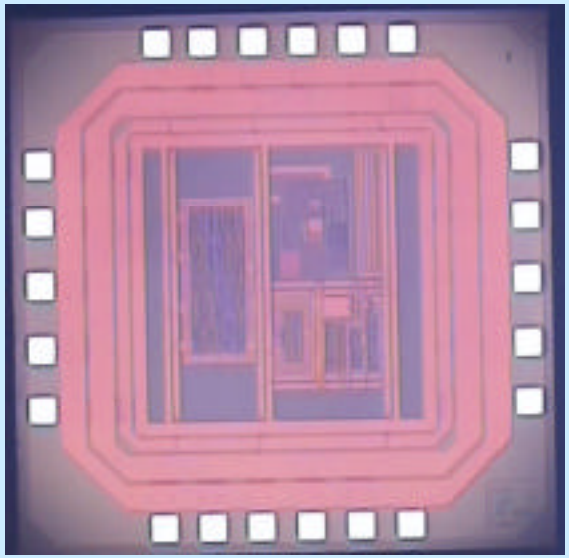




T sensor to be integrated

presently separate

test structure

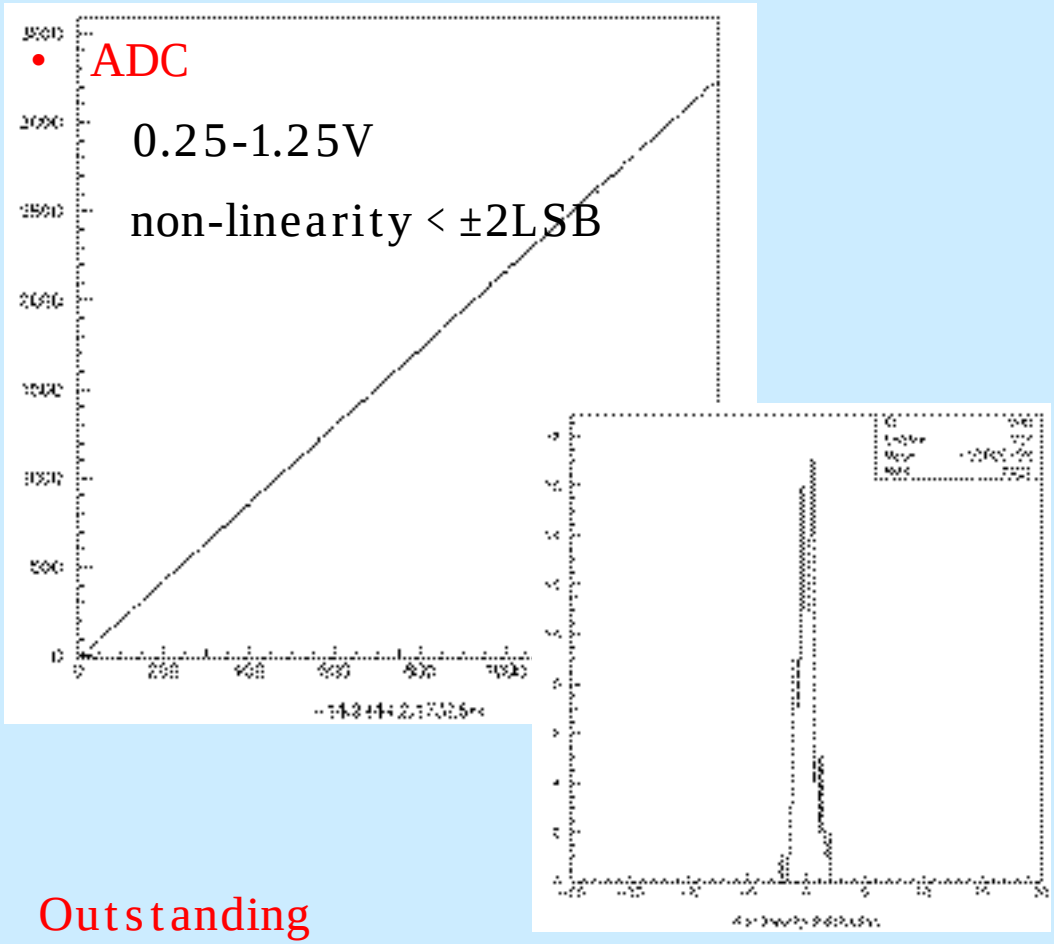


DCU performance (preliminary)

- ADC

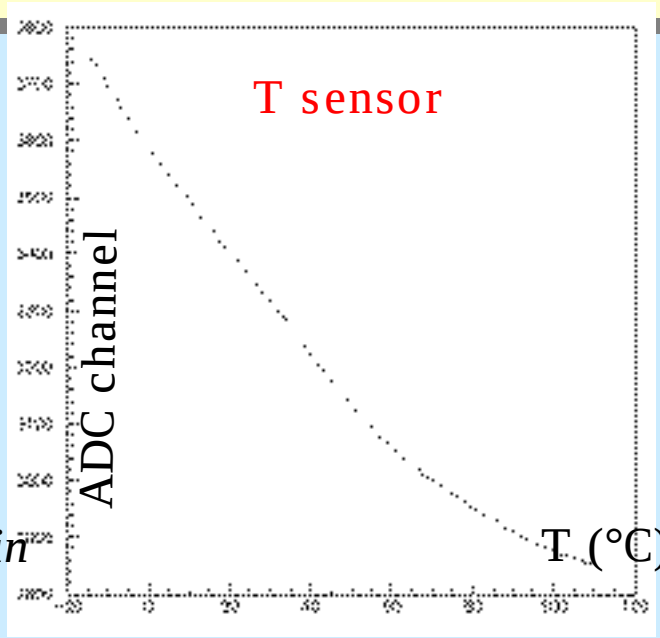
0.25-1.25V

non-linearity < ±2LSB



DCU Requirements

- Input channels: 7 (5 used)
  (+ Internal Temperature Sensing)
- Resolution: 12 bits
- INL: ±1 LSB
- DNL: no missing codes
- Conversion time: < 1ms
- Operating temperature range: -50 °C ● +50 °C
- Power Consumption: < 50 mW
- Supply Voltages: VSS = -1.25V and VDD = 1.25V
- Clock Frequency: 40 MHz (in phase with APV clock)
- Input range: GND ± 1.0V
- Die Size: 2 mm x 2 mm



- Outstanding

T sensitivity improvement?

probably adequate but final effort for extra gain

Radiation qualification

NB all CMOS hard against bulk damage

- stable process

  verify wafers within manufacturer's specs, data base to record

- stable performance

  electrical measurements of APV25 (& others)

  most statistics, detail, and prompt

NB hardness relies on
intrinsic hardness of
technology (oxide)
enclosed geometry nMOS

- total dose irradiation

  samples from 10% wafers

  APV25 & test structure in <u>both</u> UK & Padova = 20%

  x-ray, ^{60}Co, 8MeV e available

- irradiations of other components

  evidence of hardness is cumulative

NB no evidence of technology weakness
0.25µm statistics exceed
most other processes

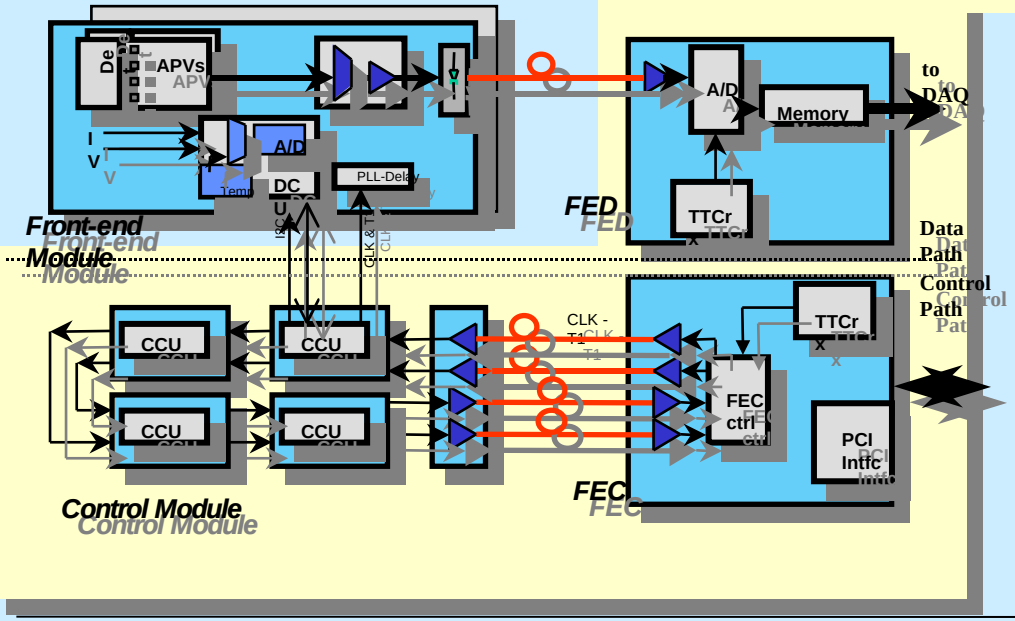
- other effects SEU, SEGR

  much data now exists, cumulative

Control system

- Non-critical path items - so far
- during 2001
  - complete ASICs
  - verify operational performance
  - plan manufacture
    - *assemble on common wafer*
    - *for cost reasons*

ASIC	Function	Status in 0.25µm	Number
CCU25	Master of control network	Rad soft version Submit 5/01	4000
LVDSMUX	Clock routing	Working	4000
LVDSBUF	Buffer	Working	10000
RX40	Digital optical receiver	Complete	1000
LD	Laser driver	Prototyped Final 5/01	20000
PLL25	Clock integrity & delay	Complete	4000



- Remaining issues are essentially:
  - cost management
  - logistics
    - *manufacture & packaging*
    - *test*
    - *assembly*
    - *QA*

Schedule ASIC chips

- APV25-S1

  10 wafers in hand ~2500 APV25

  DCU & APVMUX-PLL ok for current tests

- Final APVMUX-PLL tested September 2001

  May MPW run (=>August)

  Once proven, production masks frozen

- Further engineering run obligatory

  verify final masks

- Launch 50 wafer production - July? cost ≈ $120k

  verify large scale test procedures, data handling & storage

- Ancillary chips

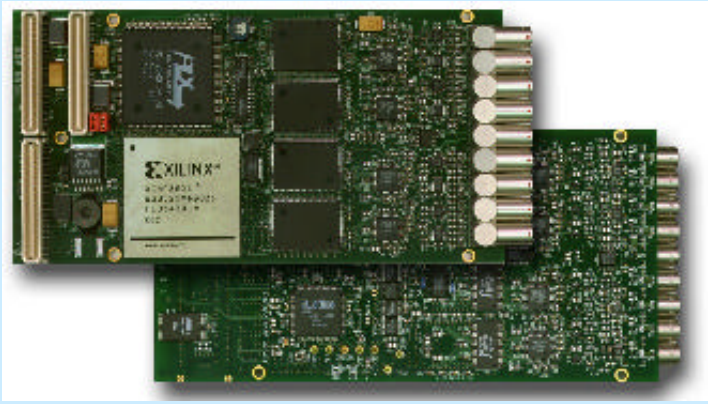
  common wafer early 2001

Sufficient for >200 modules + other tests

Front End Driver - Tracker-DAQ interface

- 8 channel PCI module in use

  ok for module testing



- Final FED - 9U VME module

  96 optical channels

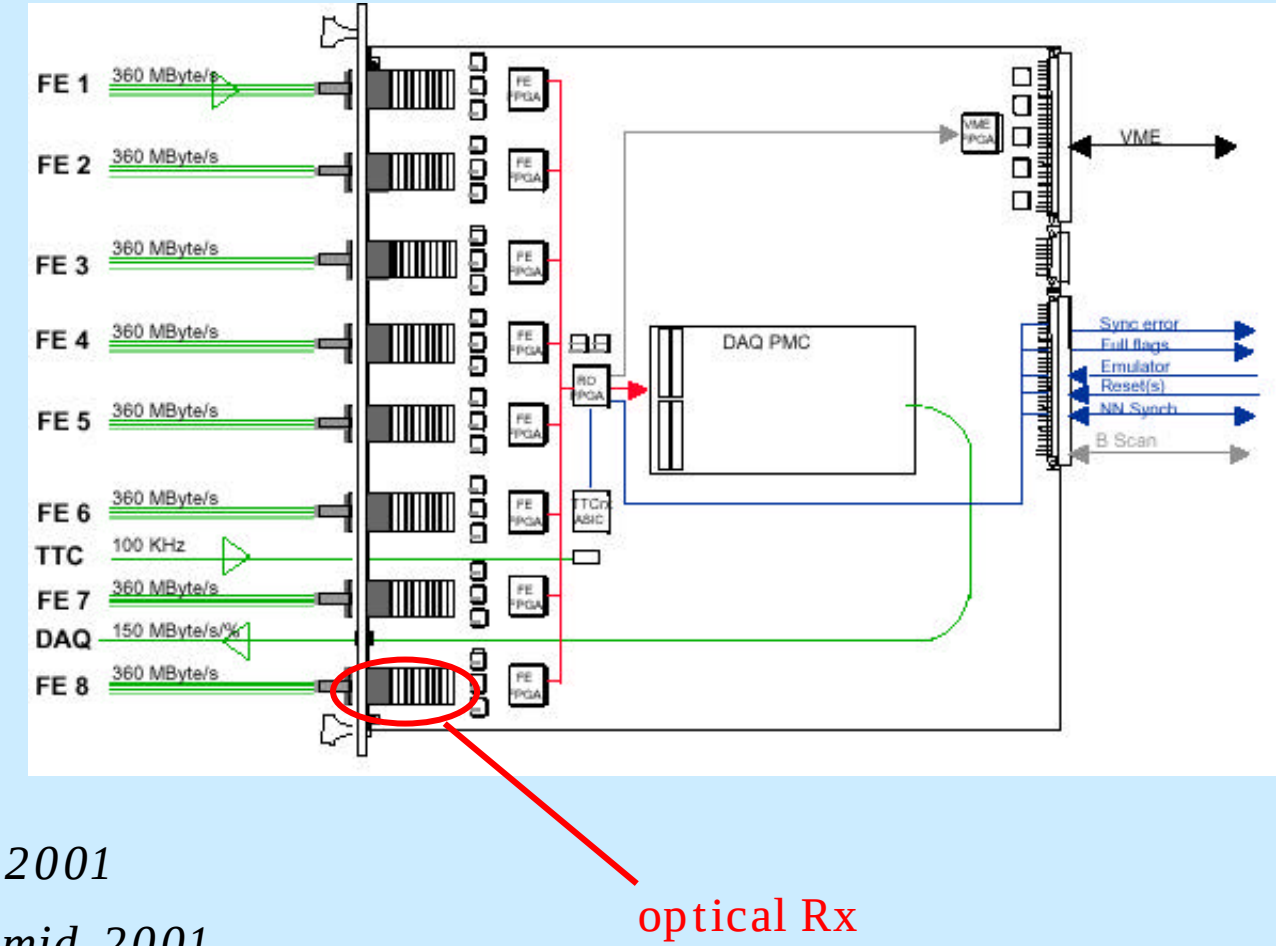
- Schedule

  design study to end 2000

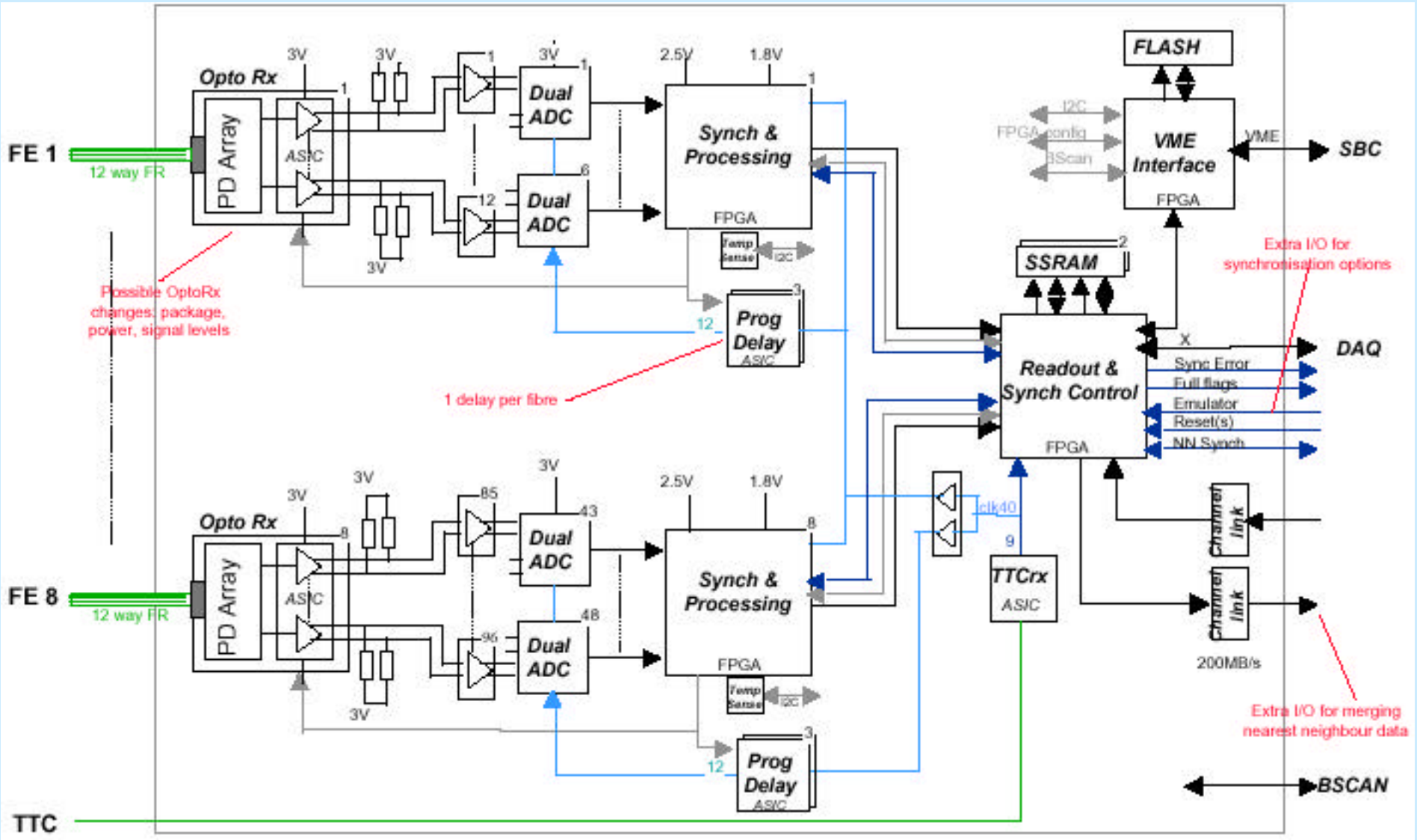
  User Requirements April 2001

  pre-production prototype mid-2001

  production match to rod/petal/IB schedule



FED functionality



Power supply system (Firenze + Torino)

- Specifications defined

- Challenging subject
  - Long cables
  - No internal regulators
  - Unbalanced I+ & I- in APV
  - Scope for noise in power delivery to module, clocks
  - ...

- System test required

July-Dec 2000	Commissioning of DAQ system.
	Cable selection and procurement.
Nov 2000:	Delivery of cables.
	Test of cable electrical specs.
Jan 2001	Delivery of power supply prototypes.
	Test of characteristics.
Feb 2001	Cables and power supply installation.
	First test of system with 1-2 detectors.
March-May 2001	Full test of system with N detectors.
	Test of different cable configurations.
June 2001	Commissioning of small scale version of system to power three groups of N detectors.
Jan 2002	Delivery of small scale version of power supply system.
Feb - May 2002	Test of whole system with three groups.
July 2002	Final cable selection and definition of the complete power supply system.
	Start cable and power supply system tendering.

Development status

- Power supplies
  - Unipolar baseline scheme adopted (0, +1.25V, +2.5V)
  - LV and HV supplies to float
  - PS modules power groups of ~60APV => ~ 1800 PS units
  - *Cost model vs current to be provided*

- Cables *3 major sections*
  - *USC55 - detector racks ~100m*
  - *Detector racks - patch panel ~40m*
  - *Patch panel - module groups 4-5m*
  - preliminary costings exist, more detailed quotes to be obtained

- Open questions
  - detailed module grouping
  - cost and time implications of any problems

LHC-like beam test May 2000

- **Motivation**

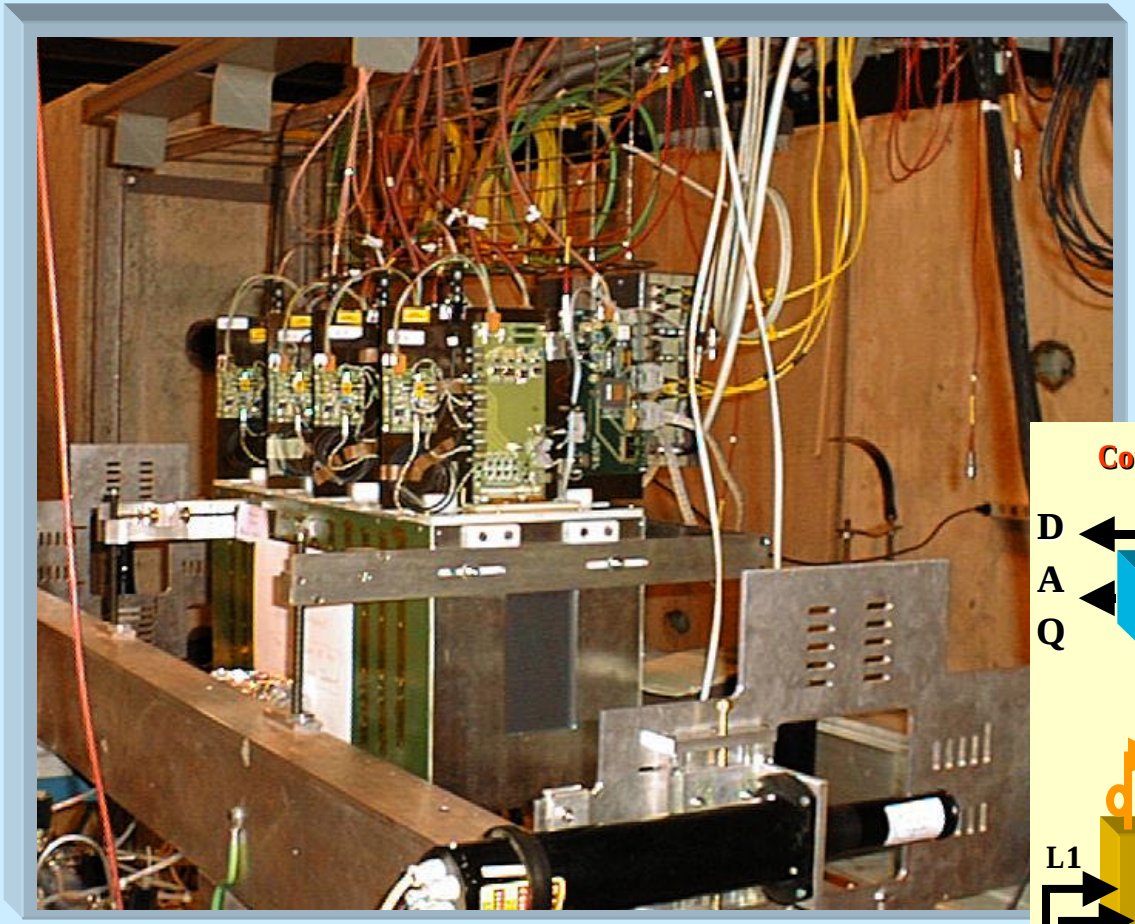
Operate in an LHC like environment a tracker electronics chain:

- FE read-out — APV chips
- Control system — FEC + CCUs + PLLs
- Data Acquisition: — FEDs
- Optical Links — digital for timing and control; analogue for data transfer

Debug the system and start answering questions such as:

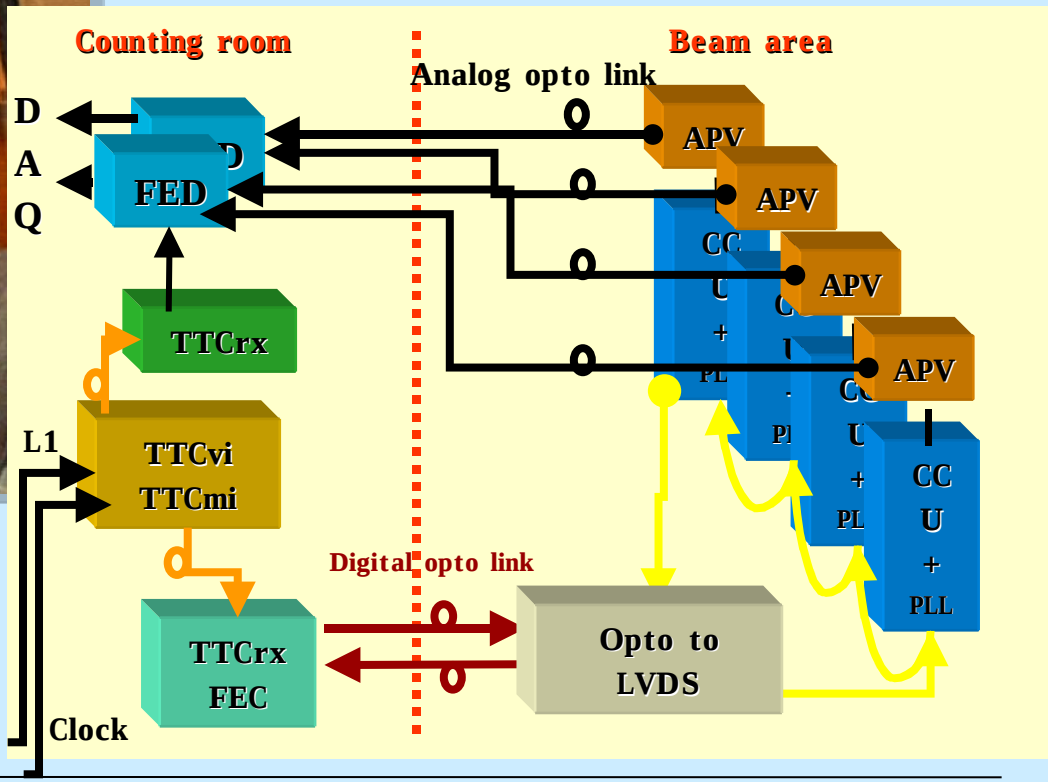
- How to synchronise a modest number of detectors?
- Effect from close triggers on the data quality ?
- How long system can run continuously in an LHC like environment?
- + many others...

X5 setup



NB APV6

- Successful proof of system
- Now upgrade to APV25 & 0.25µm



Conclusions from 25ns beam test

- Successful CCU control of I2C devices

  APV, PLL, laser drivers and T sensors

- System successfully synchronised

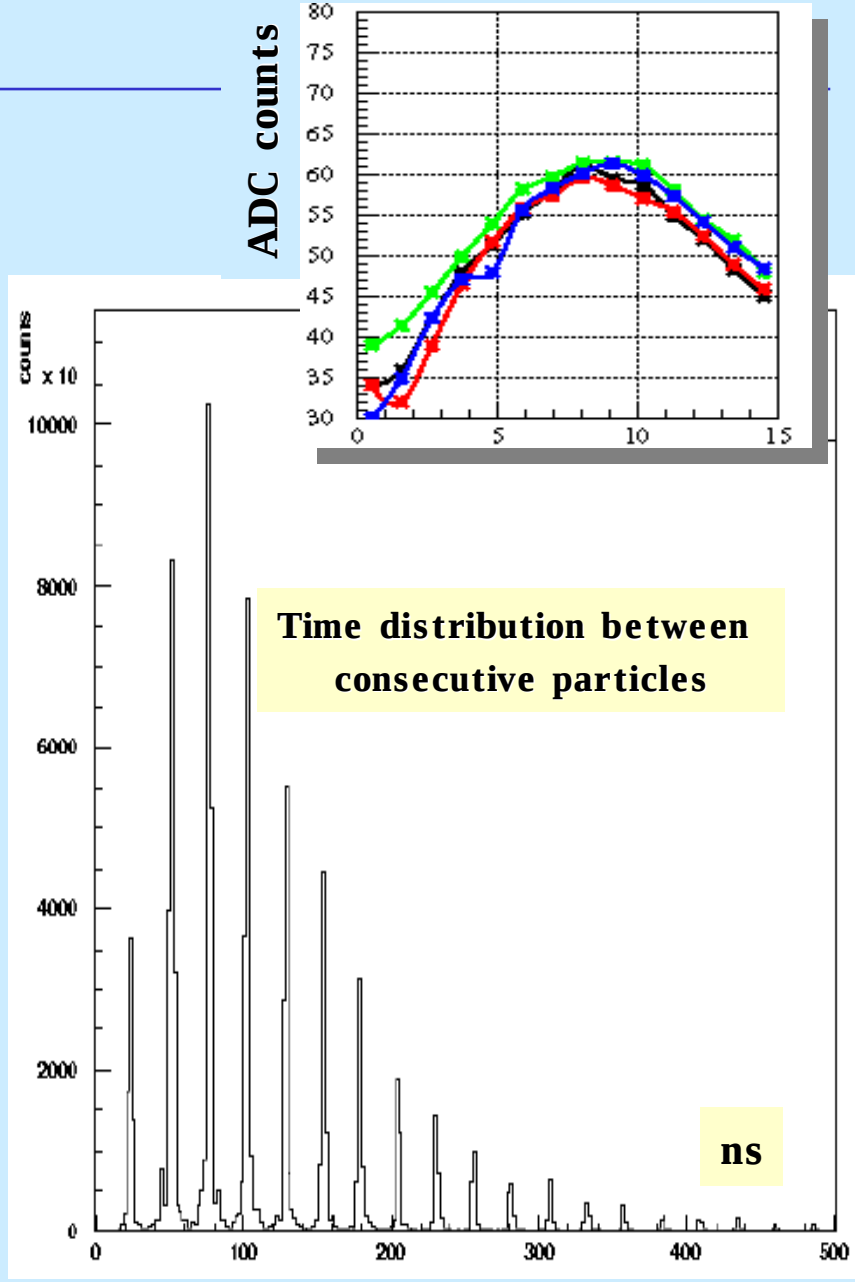
  automatic scheme being developed

- Integration of analogue and digital optical links

- Max CMS rates - *for short bursts*

  Data with 1001 & other triggers

- **25ns beam essential tool for system studies**



Preparations for 2001 system test

- Stages
  - System software and hardware
    - *well advanced*
  - Final hybrid assembly and operation
    - *working hybrid operational*
  - Module assembly and operation
  - Multi-module installation
  - Operation of TOB rod
    - *subsequently TEC & TIB units*
- + several internal reviews
  - *ASIC final review*
  - *FE hybrid*
  - *Power & grounding*
  - *DAQ & Control system*

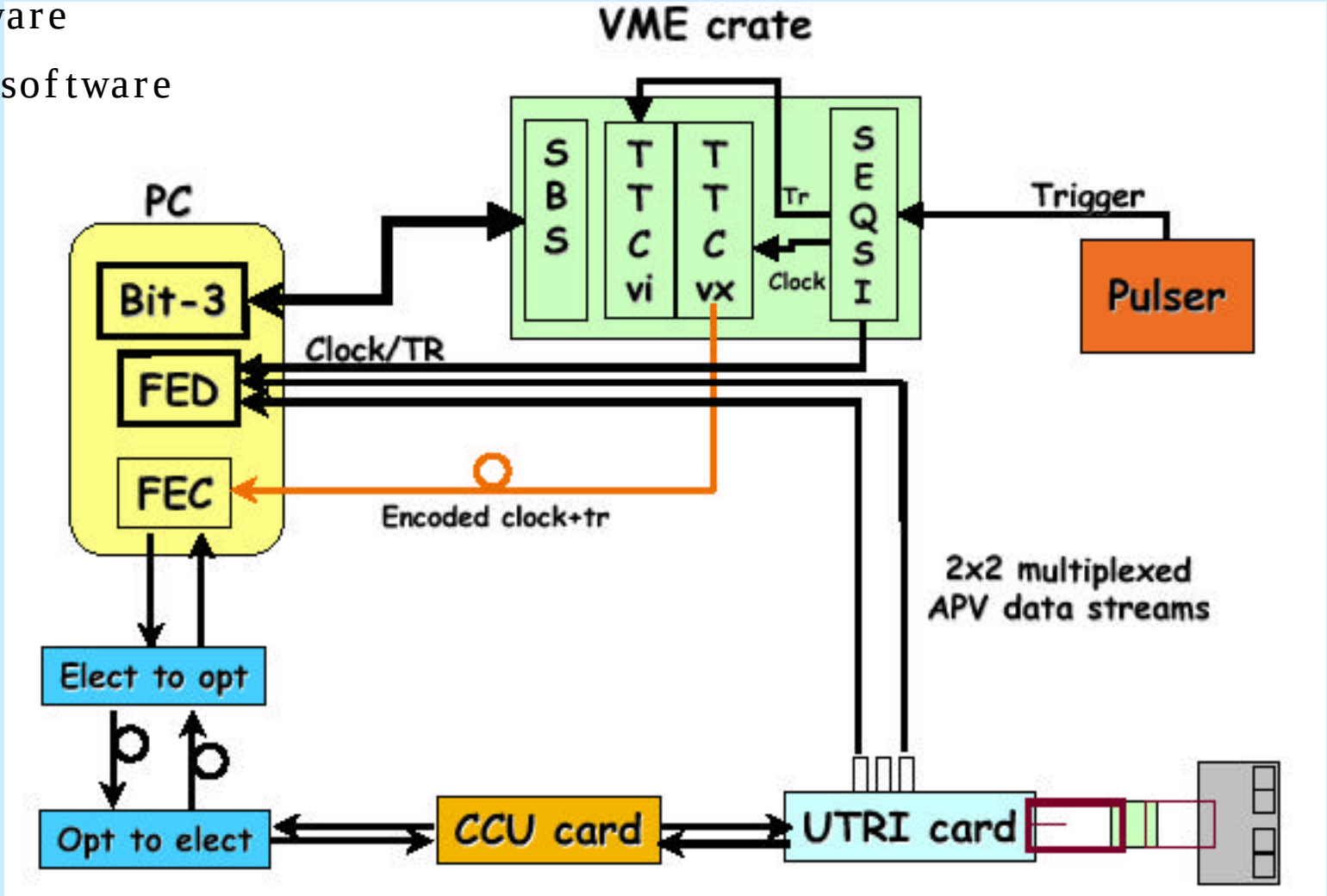
Aim to complete system test and hold ESR in December 2001

PC based test-bench at CERN

- Symbiosis between module test set-up and system test

  common hardware

  much common software



Summary

- All component developments virtually complete
  - Performance, power, size, *cost* well understood
  - Radiation performance & robustness proven
  - FE ASIC testing systems & radiation qualification equipment in place
- Power supplies and cabling now under way
- System test advancing steadily
  - schedule aggressive but no major obstacles foreseen
- Remaining risks
  - costs — *need to complete optical tender to manage*
  - technical — *associated with component assembly and QA*
- Production - *large scale orders: begin after December 2001 (& ESR)*
  - Milestone 200 & rod test provides final verification