The Opto- hybrid tester:

The goals:

Test the different analog opto-hybrid devices

Test the digital opto-hybrid device

Test continuity of an optical line

Presentation:

A box of 30 x 20 cm 11 height

Inside the box: (page 2)

2 printed circuits

1 power supply

1 Optical head

1 LVDS head

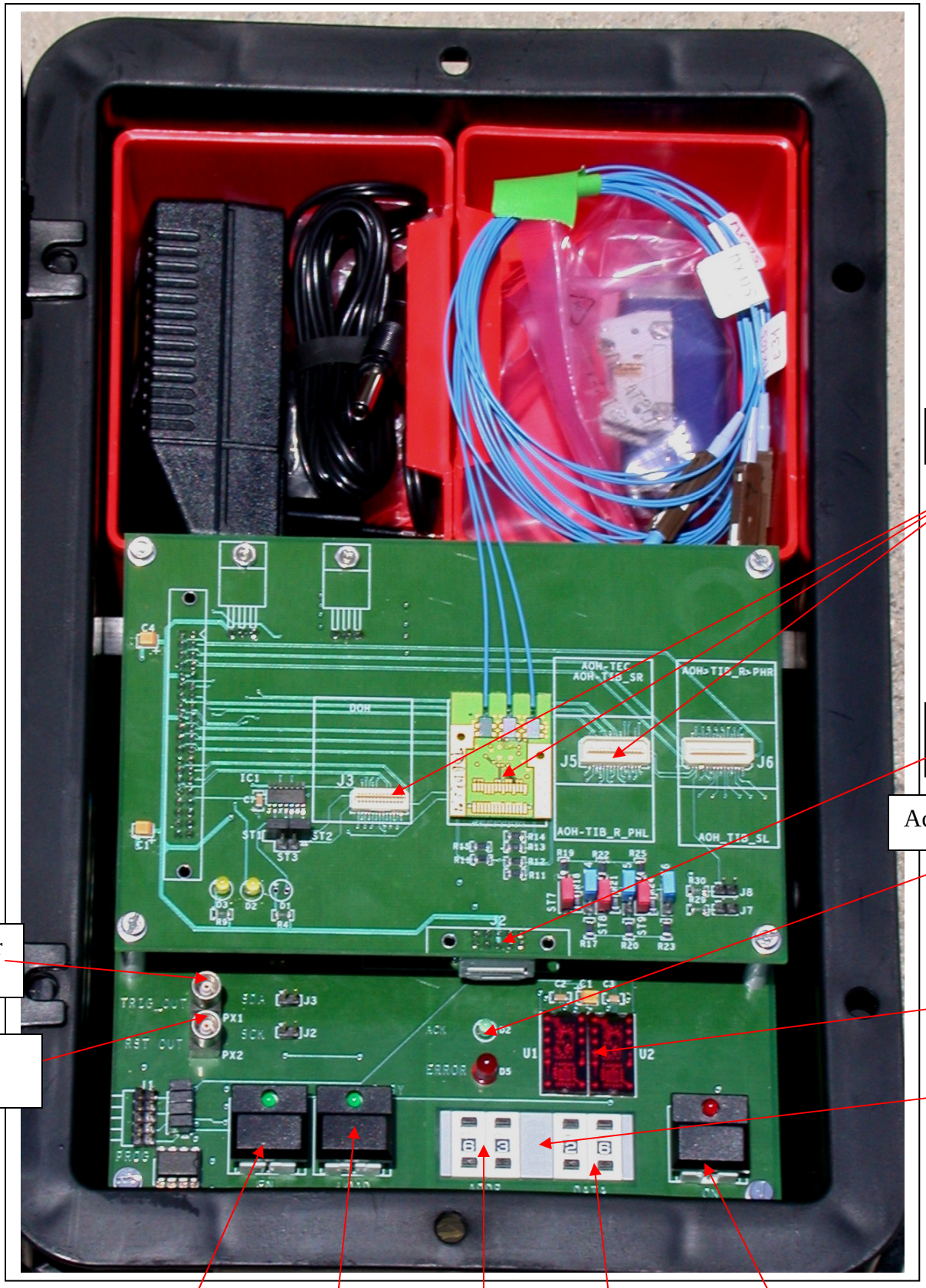
1 light pen (Visual Fault Locator)

1 flat cable

Power supply

Optical head

LVDS head



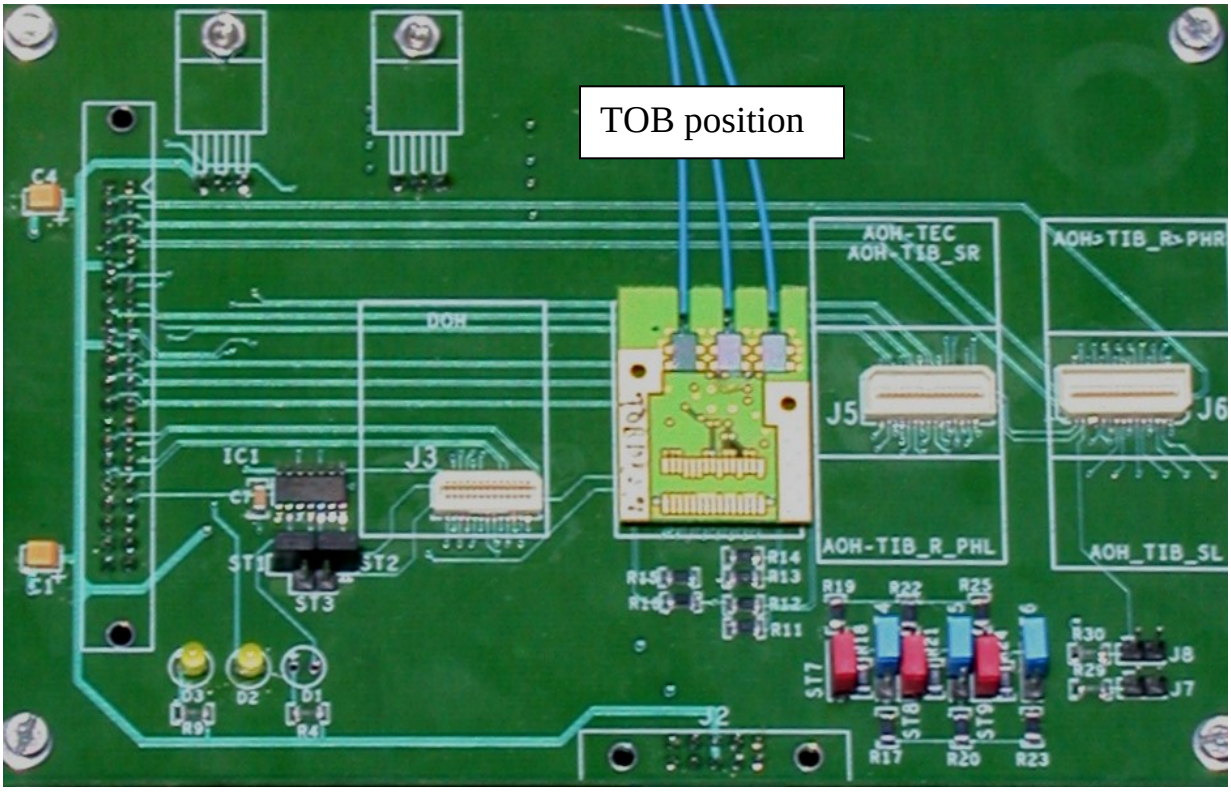
1-Analog opto-hybrid testing device:

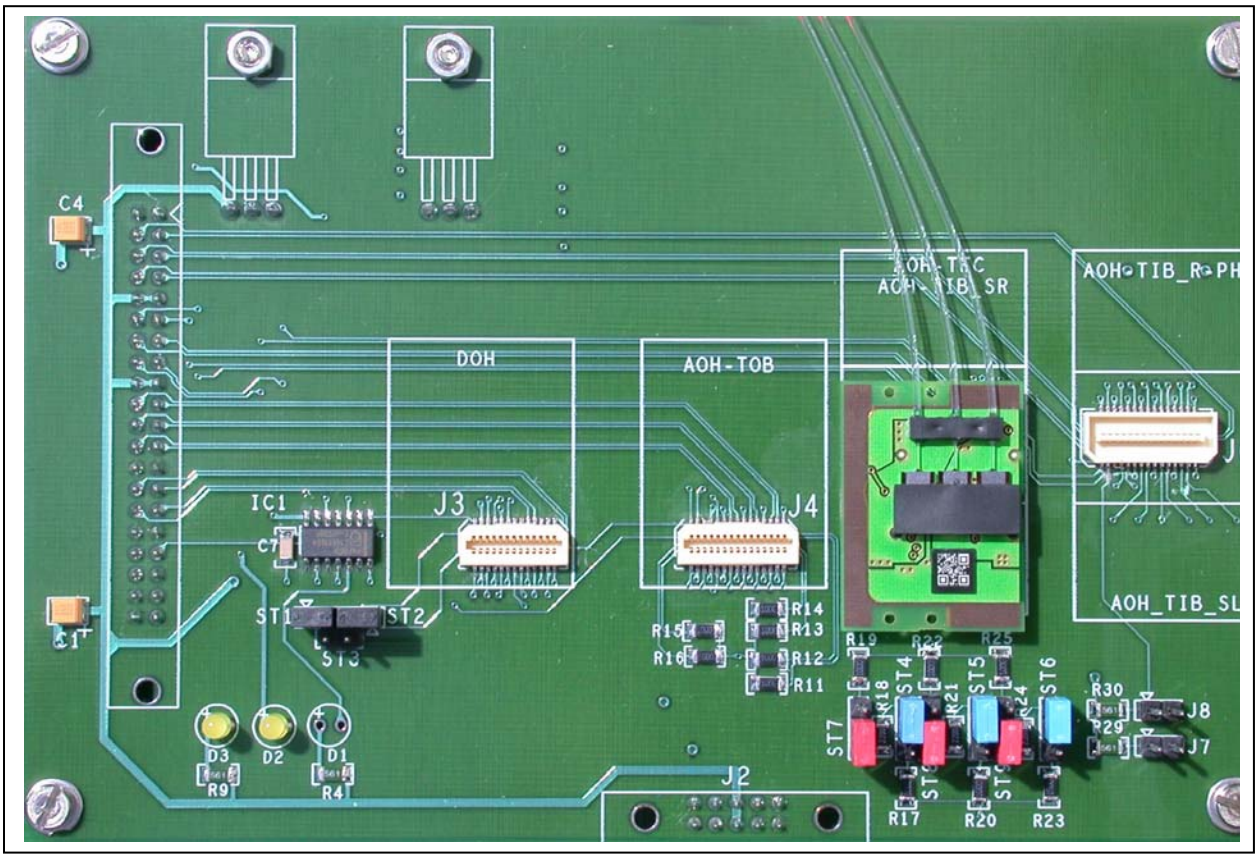
First of all, make sure the power is OFF: (Lower-right button in figure on page 2)

You **should** be wearing an EMC bracelet!

Locate the AOH device on the correct connector. If you are using the J5 connector, please adjust the correct impedance through the jumpers (ST4, ST5, ST6, ST7, ST8, ST9).Page 4 and 5.

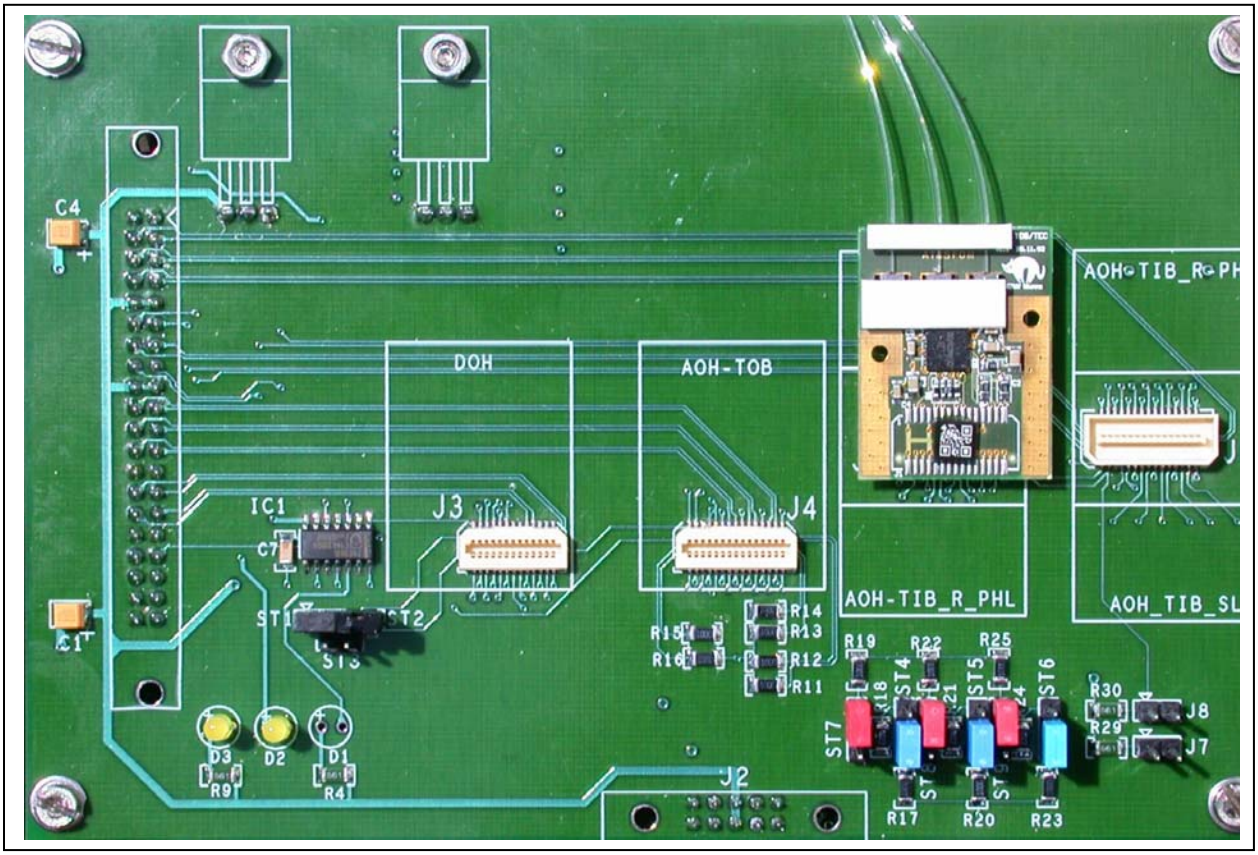
See the following pictures





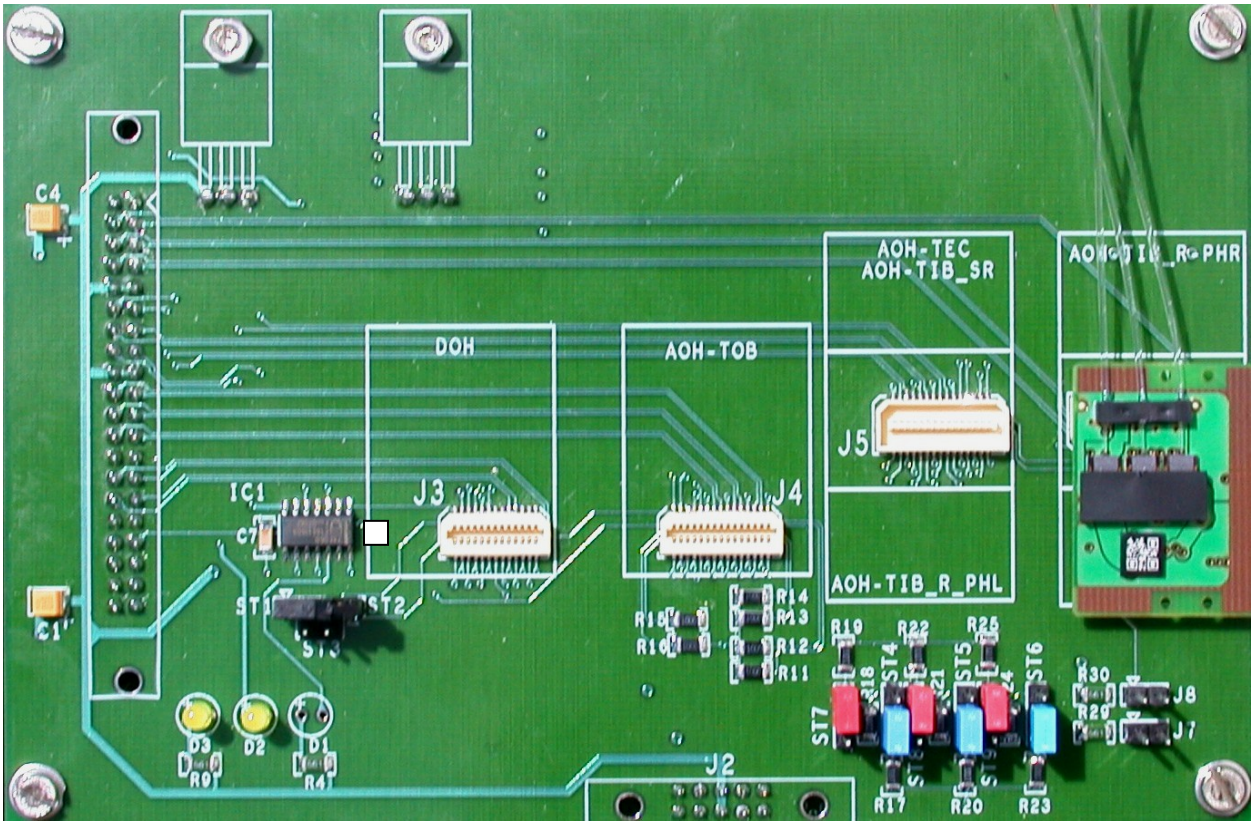
TIB-R-PHL position

Jumpers in position: 220 ohms

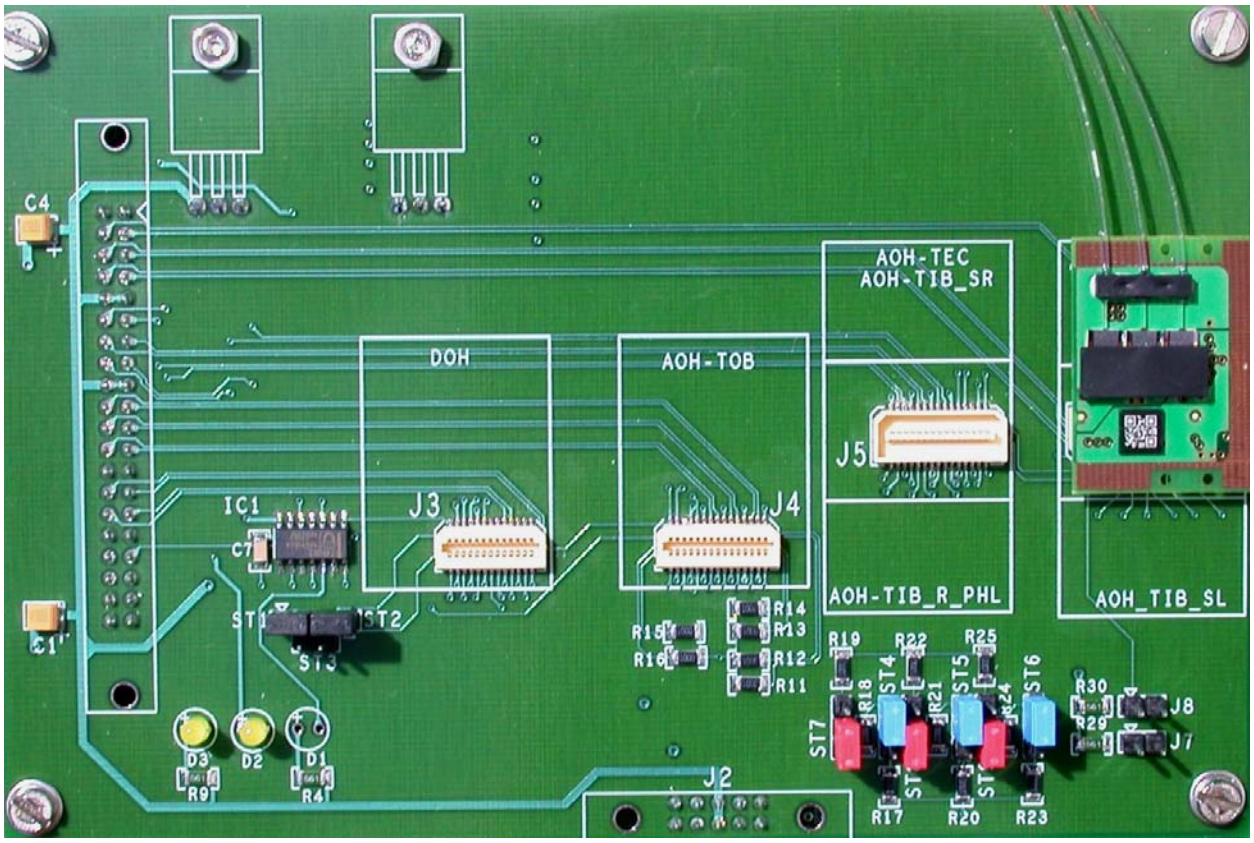


TEC

AOH-TIB-SR


C4
DOH
AOH-TOB
AOH-TEC
AOH-TIB_SR
J5
J3
J4
IC1
C7
C1
ST1
ST2
ST3
AOH-TIB_R_PHL
R14
R13
R12
R11
R19
R22
R25
ST4
ST5
ST6
ST7
R30
R29
J8
J7
D3
D2
D1
R9
R4
J2
R17
R20
R23

TIB-SL



TIB-R-SL

Jumpers in position 2x 110 ohms

At power-up, the system performs some hidden tasks for you:

1- It configures the FPGA
2- It sets the bias current of the laser diodes
   At the address 60 the register value will be 20
   At the address 61 the register value will be 20
   At the address 62 the register value will be 20

The system is now ready to put at what address you want the value you want through the I2C protocol.
The 2 left coded wheels encode the (hexadecimal) address value.
The 2 right coded wheels encode the (hexadecimal) data value.

Remark 1:

For an AOH, address (hex)60 corresponds the right-most fibre-channel. This channel is modulated with a 10 MHz square wave. This is referred to as channel 1 below.
For an AOH, address (hex)61 corresponds the central fibre-channel. This channel is modulated with a 20 MHz square wave. This is referred to as channel 2 below.
For an AOH, address (hex)62 corresponds the left-most fibre-channel. This channel is modulated with a 40 MHz square wave. This is referred to as channel 3 below.
Using different modulation frequencies on the different channels allows the channels to be identified without the need for a 2D-code reader.

Remark 2:

Expert people can skip this remark and jump to the" operation chapter".
For non expert people, please just play with the following values.
At the address 63, you can set the gain of the device. Try the following values:
"63-00" This value will set the gain 0 on the channel 1.
"63-01" This value will set the gain 1 on the channel 1.
"63-02" This value will set the gain 2 on the channel 1.
"63-03" This value will set the gain 3 on the channel 1.

"63-00" This value will set the gain 0 on the channel 2.
"63-04" This value will set the gain 1 on the channel 2.
"63-08" This value will set the gain 2 on the channel 2.
"63-0C" This value will set the gain 3 on the channel 2.

"63-00" This value will set the gain 0 on the channel 3.
"63-10" This value will set the gain 1 on the channel 3.
"63-20" This value will set the gain 2 on the channel 3.
"63-30" This value will set the gain 3 on the channel 3.

Operations:

Connect one optical channel to the optical head (50 mV, 50 ohms)
Push the “LOAD” button (refer to the remark 1)
The light D2 also noted “ACK” will tell you about the result of the I2C transaction
The light is green; the device had sent back an acknowledgement to the transaction.
In this case, you can see on the 2 hexadecimal displays the value of the data the device sent you back. This value should be the value you sent
The light remains off; the device didn’t recognize the address.
In this case, the 2 hexadecimal displays show you “FF”.
About The enable button:
If enable (light button green) the modulation is applied on the 3 channels
If not enable (no light button) the modulation is not applied on the 3 channels and you see the bias current level (remember the default setting is 20).

Operation details:

Hereby, an expert will get more explanations on how the system works.

At the power up, the FPGA (ALTERA EPF 10K10LC84-4) will be initialized through an EP1441 (left down the PCB).

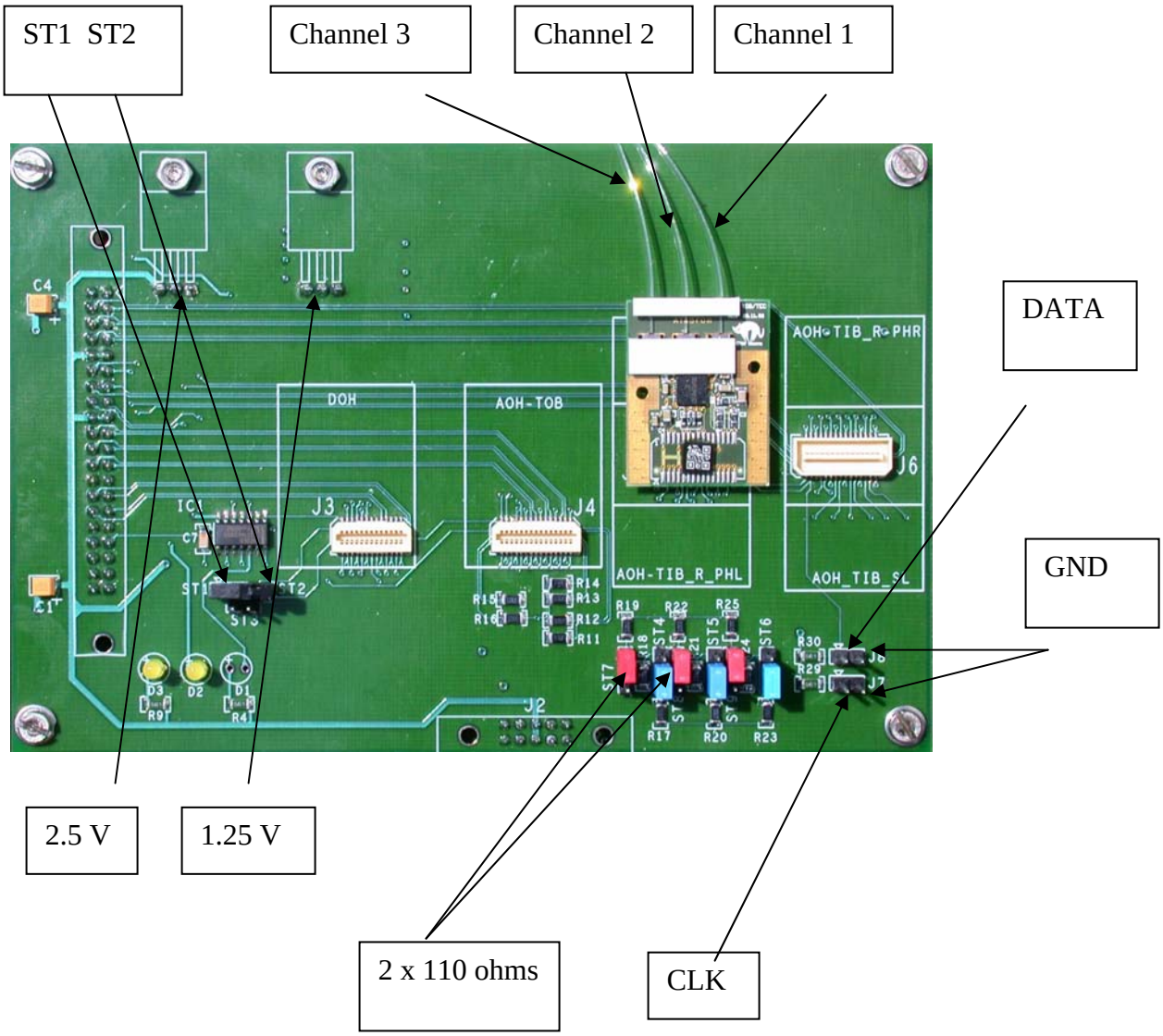
After this cycle, the initialization of the device has been done (3 write cycles) as defined on the previous chapter.

At this time starts the test cycle, it means that a write **and** a read cycle are performed successively on each “LOAD” request. The system doesn’t take the “acknowledge” signal into account, it just show you if the device “understand” the address you perform in highlighting the green light D2 also called ”ACK”. You can scope the I2C lines on J8 (data) and J7 (clock).

Pushing down the “load” button permanently will generate “LOAD” cycle in sequence.

Removing the straps ST1 and ST2 allows you to get access to the I2C lines in isolating these lines from the system. It is up to you to there connect your own I2C line giving you the possibility to connect a PC driving system. This way the system will only drive the analog line.

Separated I2C (clk and data) signal can be scope on the pins J2 and J3.


ST1 ST2
Channel 3
Channel 2
Channel 1
DATA
GND
2.5 V
1.25 V
2 x 110 ohms
CLK
DOH
AOH-TOB
AOH-TIB_R_PHL
J2
J3
J4
J6
J7
ST1
ST2
ST4
ST5
ST6
ST7

Digital opto-hybrid testing device:

Remark 1:

As not everybody will test the DOH devices, and because of the availability of the component, the MU-MU connectors necessary to inject the optical output signals in the optical receivers will be distributed on request only.

Remark 2:

The device will not “answer” on his addresses if it is on reset mode. This can be seen on the LEMO plug PX2 also called “RST OUT”.

The reset mode happens if no signal is apply on the data line.

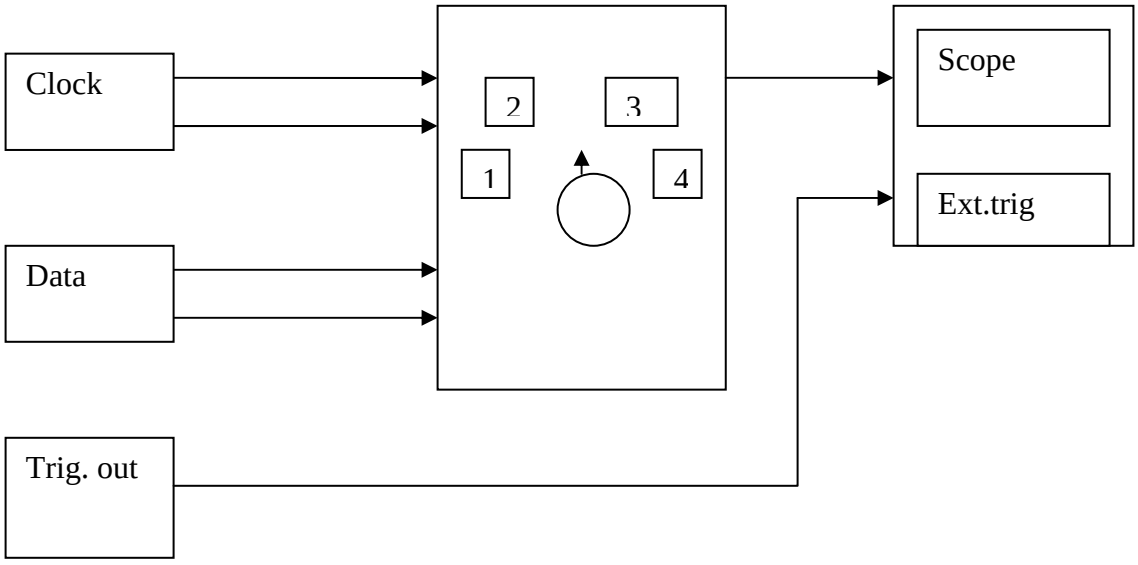
Remark 3:

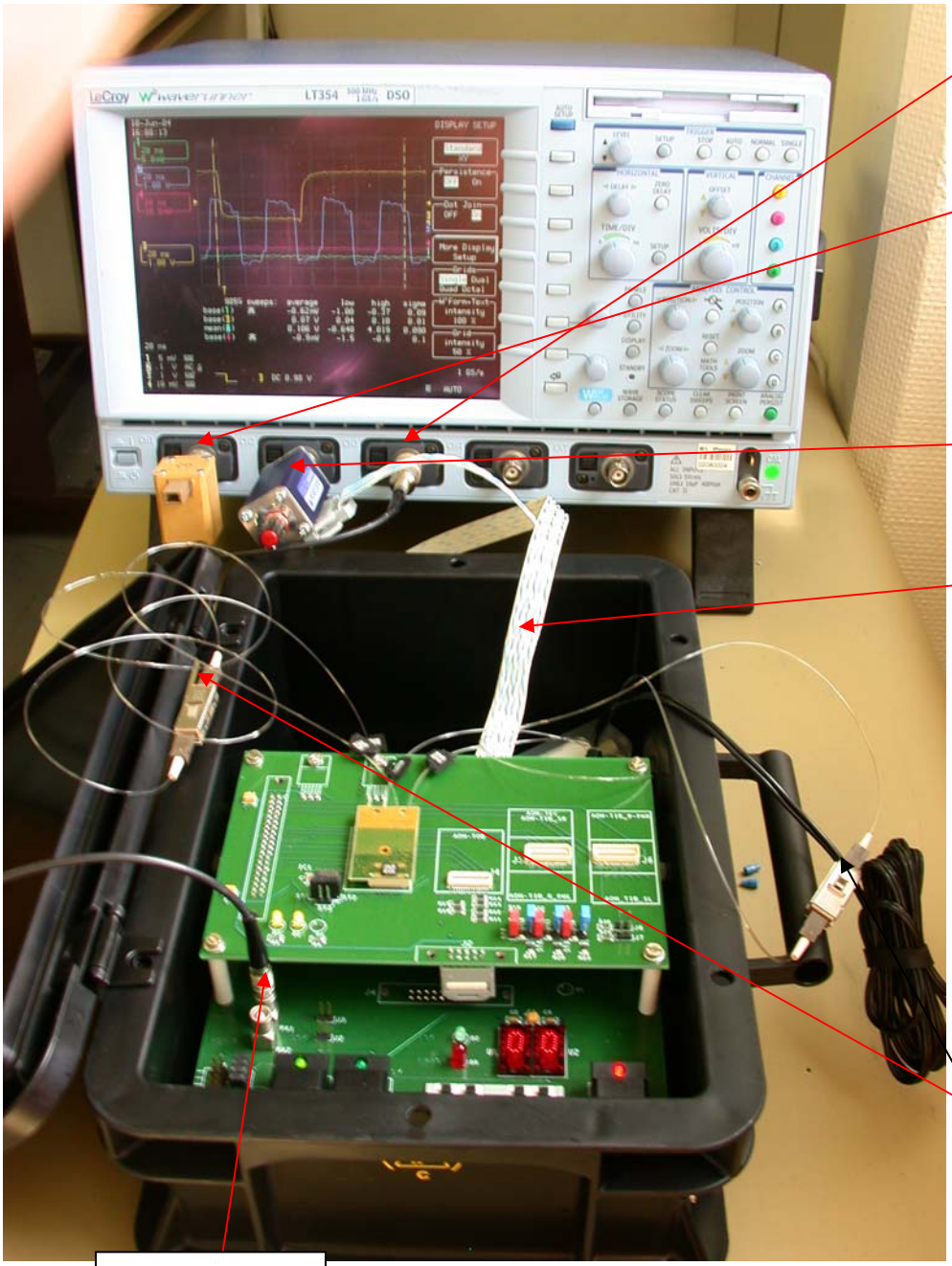
There is a bias current default setting (maximum) for each laser diode at the address 70 and 72.

Have a look on the setup at page 13 and 14

About the scope, the LVDS like signal has to be read on an AC input on 1 Mohm.

The rotating button will show you the 2 LVDS channels each of them has been reported on 2 different outputs. Page 12 will show you the schematic.


Clock
Data
Trig. out
2
3
1
4
Scope
Ext.trig


Syn. cable
Optical head
LVDS probe
LVDS cable
MU-MU connectors
Trigger Output

Trig. out

Modulated signal

Operation:

Have a look on a DOH, The two left fibres are the laser diodes and the two right fibre are the receiver channels.

The first thing to do to avoid the reset condition is to connect the output fibres to the input fibres by the mean of two MU connectors as shown on the page 12.

Enable the modulation in getting a green light on the enable button

At this time the DOH leave the reset mode in validating the RST OUT output. In disabling the button “EN”, you suppress the modulation and the circuit comes back to the reset mode. The same condition can be get in interrupting the data optical link.
By the way, only interrupting the clock link will leave alive the device.

In activated mode, you can now verify the device answers an I2C transaction as an AOH device.

You can scope the 2 LVDS channels on the LVDS head (page 16, 17, 18,19.

In using a dedicate synchronization on your scope you will manage to measure the number of cycle the device took to redirect a reset signal (typically 10 cycles).

Contact:

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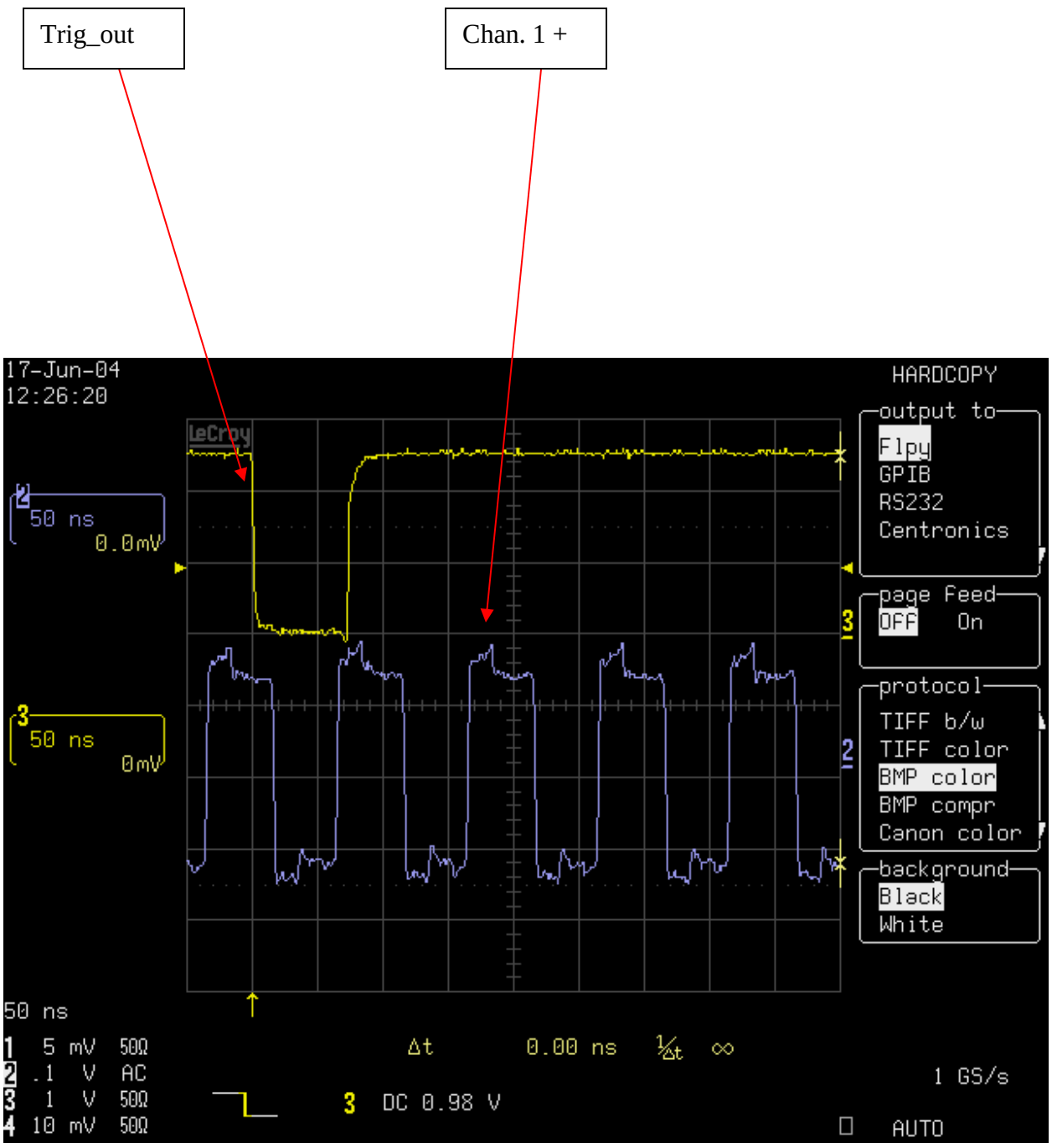
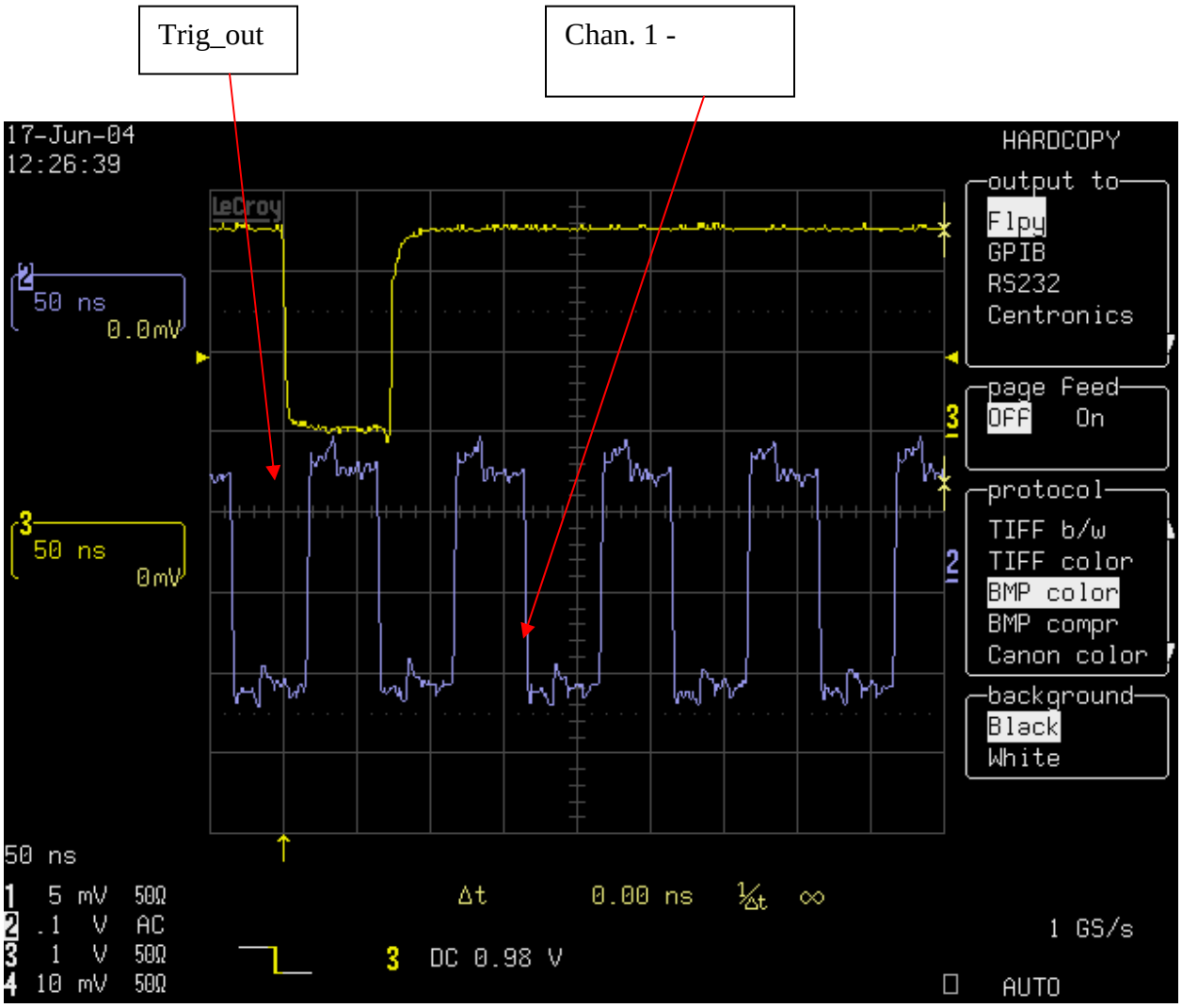
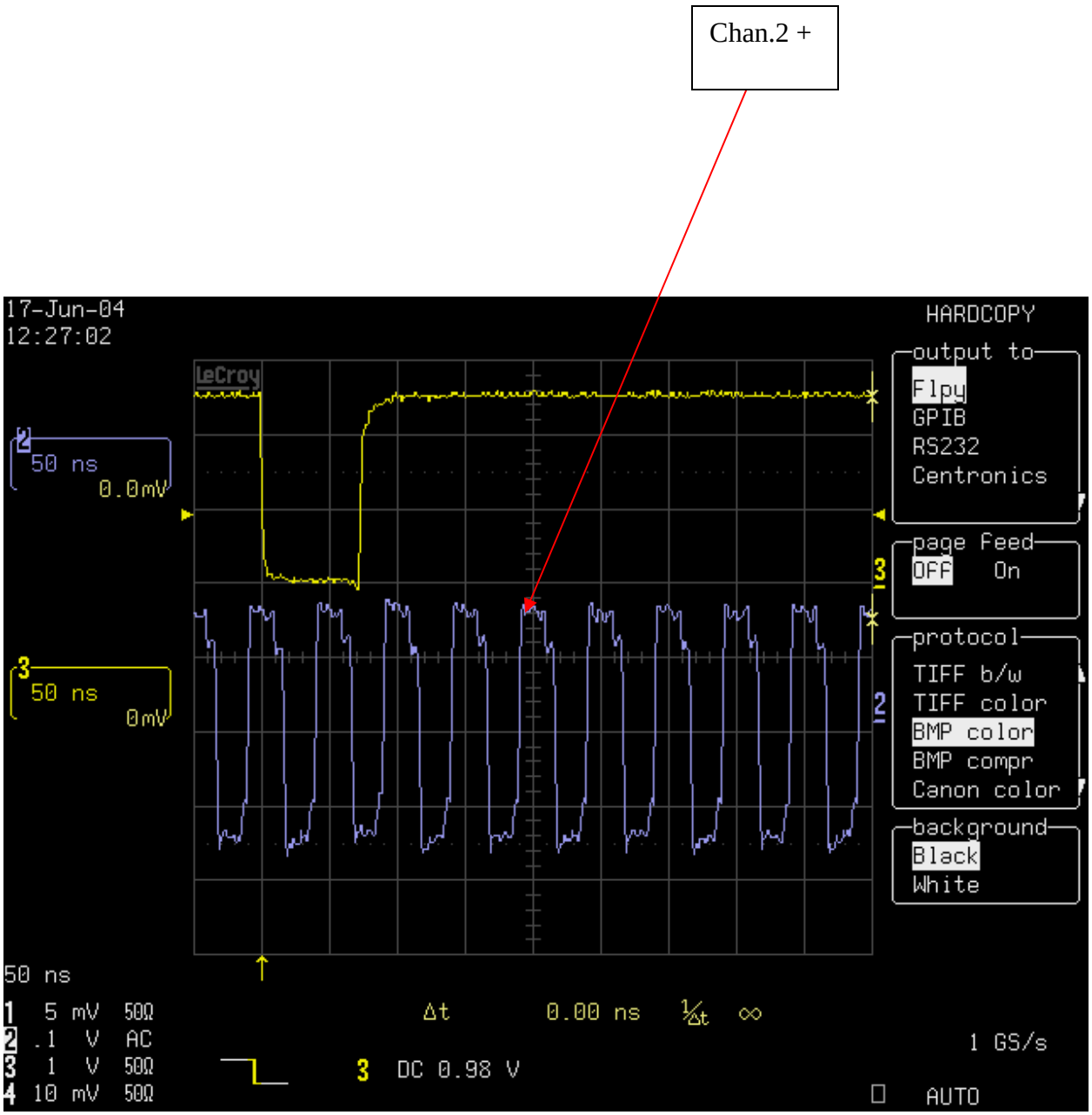
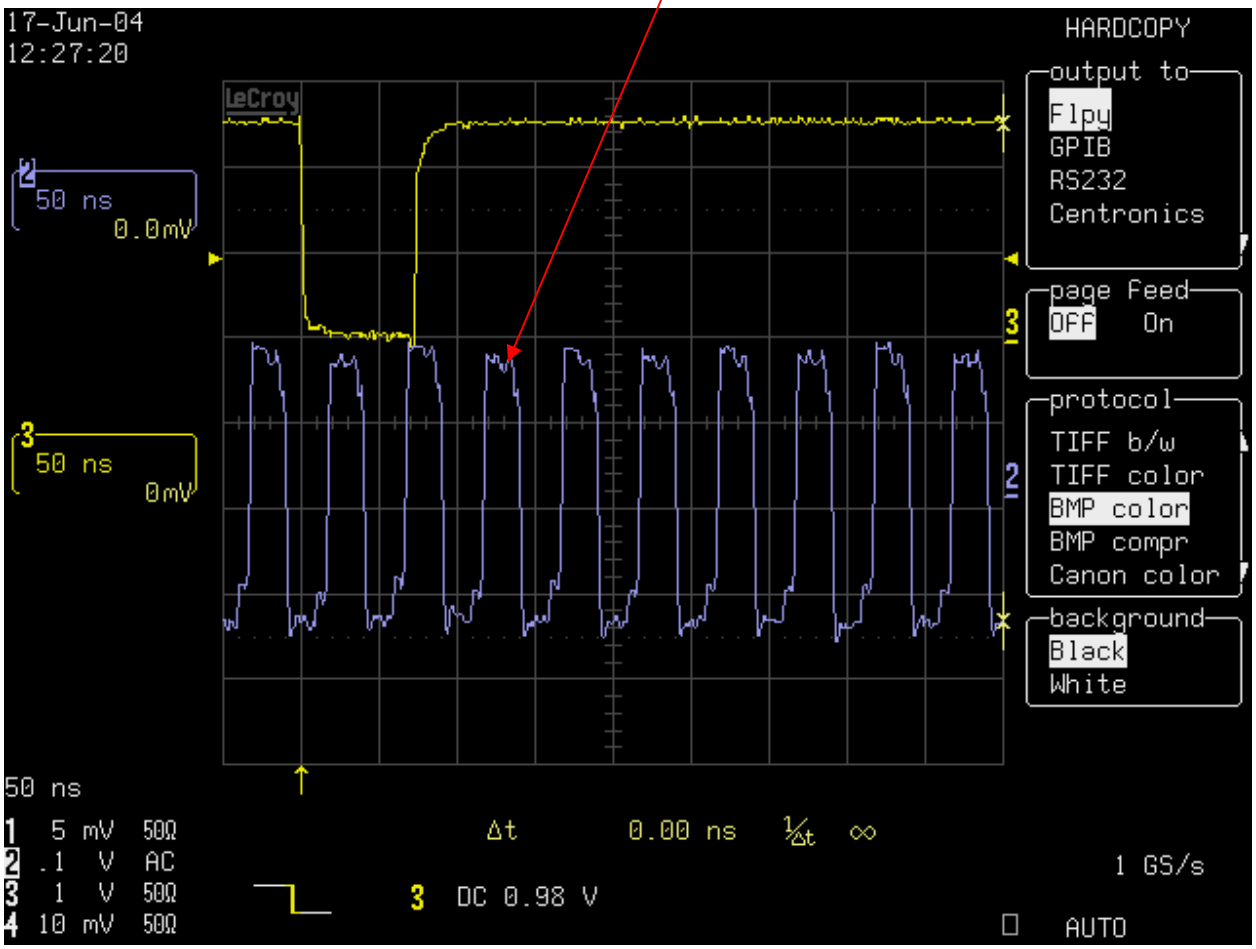

Trig_out
Chan. 1 +
17-Jun-04
12:26:20
HARDCOPY
output to
Flpy
GPIB
RS232
Centronics
page Feed
OFF
On
protocol
TIFF b/w
TIFF color
BMP color
BMP compr
Canon color
background
Black
White
LeCroy
2
50 ns
0.0mV
3
50 ns
0mV
50 ns
1 5 mV 50Ω
2 .1 V AC
3 1 V 50Ω
4 10 mV 50Ω
Δt 0.00 ns 1/Δt ∞
3 DC 0.98 V
1 GS/s
AUTO


Trig_out
Chan. 1 -
17-Jun-04
12:26:39
HARDCOPY
output to
Flpy
GPIB
RS232
Centronics
page Feed
OFF
On
protocol
TIFF b/w
TIFF color
BMP color
BMP compr
Canon color
background
Black
White
LeCroy
50 ns
0.0mV
50 ns
0mV
50 ns
1 5 mV 50Ω
2 .1 V AC
3 1 V 50Ω
4 10 mV 50Ω
Δt 0.00 ns
1 GS/s
3 DC 0.98 V
AUTO


Chan.2 +
17-Jun-04
12:27:02
LeCroy
HARDCOPY
output to
Flpy
GPIB
RS232
Centronics
page Feed
OFF
On
protocol
TIFF b/w
TIFF color
BMP color
BMP compr
Canon color
background
Black
White
50 ns
0.0mV
3
50 ns
0mV
50 ns
1 5 mV 50Ω
2 .1 V AC
3 1 V 50Ω
4 10 mV 50Ω
Δt 0.00 ns 1/Δt ∞
3 DC 0.98 V
1 GS/s
AUTO

Chan. 2 -


17-Jun-04
12:27:20
HARDCOPY
output to
Flpy
GPIB
RS232
Centronics
page Feed
OFF
On
protocol
TIFF b/w
TIFF color
BMP color
BMP compr
Canon color
background
Black
White
LeCroy
2
50 ns
0.0mV
3
50 ns
0mV
50 ns
1 5 mV 50Ω
2 .1 V AC
3 1 V 50Ω
4 10 mV 50Ω
Δt 0.00 ns 1/Δt ∞
3 DC 0.98 V
1 GS/s
AUTO